



iVPI



Integrated  
Vital Processor  
Interlocking Control  
System

Non-Vital Subsystem

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Non-Vital Subsystem Manual  
**P2521B, Volume 4**





iVPI



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Vital Processor  
Interlocking Control  
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Non-Vital Subsystem

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Non-Vital Subsystem Manual  
**Alstom Signaling Inc.**

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**PREFACE**

**NOTICE OF CONFIDENTIAL INFORMATION**

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## **ABOUT THE MANUAL**

This manual is intended to describe the Alstom Integrated Vital Processor Interlocking Control System, (iVPI) non-vital subsystem (non-vital boards). This manual is part of a 5 volume set of manuals. The set is summarized in Section 1.

The information in this manual is arranged into sections. The title and a brief description of each section follow:

**Section 1 – NON-VITAL SUBSYSTEM:** This section summarizes the iVPI non-vital subsystem boards.

**Section 2 – NVSP (NON-VITAL SYSTEM PROCESSOR) BOARD, P/N 31166-428-XX:** This section provides NVSP board detail.

**Section 3 – NVI (NON-VITAL INPUT) BOARD, P/N 31166-457-XX:** This section provides NVI board detail.

**Section 4 – NVO (NON-VITAL OUTPUT) BOARD, P/N 31166-458-XX:** This section provides NVO board detail.

**Section 5 – NVSP INTERFACE BOARDS, P/N 31166-474-XX, 31166-475-XX:** This section provides NVSP Interface board detail.

**Appendix A – NON-VITAL BOARD LAYOUT DRAWINGS:** This section provides the layout drawings the non-vital boards.

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## **MANUAL SPECIAL NOTATIONS**

In the Alstom manuals, there are three methods used to convey special informational notations to the reader. These notations are warnings, cautions, and notes. Both warnings and cautions are readily noticeable by boldface type two lines beneath the caption.

### Warning

A warning is the most important notation to heed. A warning is used to tell the reader that special attention needs to be paid to the message because if the instructions or advice is not followed when working on the equipment then the result could be either serious harm or death. The sudden, unexpected operation of a switch machine, for example, or the technician contacting the third rail could lead to personal injury or death. An example of a typical warning notice follows:

#### **WARNING**

DISCONNECT MOTOR ENERGY WHENEVER WORKING ON SWITCH LAYOUT OR SWITCH MACHINE. UNEXPECTED OPERATION OF MACHINE COULD CAUSE INJURY FROM OPEN GEARS, ELECTRICAL SHOCK, OR MOVING SWITCH POINTS.

### Caution

A caution statement is used when an operating or maintenance procedure, practice, condition, or statement, which if not strictly adhered to, could result in damage to or destruction of equipment. A typical caution found in a manual is as follows:

#### **CAUTION**

Turn power off before attempting to remove or insert circuit boards into a module. Boards can be damaged if power is not turned off.

### Note

A note is normally used to provide minor additional information to the reader to explain the reason for a given step in a test procedure or to just provide a background detail. An example of the use of a note follows:

#### **NOTE**

A capacitor may be mounted on the circuit board with a RTV adhesive. Use the same color RTV.

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# 1. SECTION 1 – NON-VITAL PRINTED CIRCUIT BOARDS

## 1.1. INTRODUCTION

This manual describes the Printed Circuit Boards used to provide non-vital functionality in the iVPI System.

See P2521B, Volume 2, Table 2–1, for the Vital and Non-Vital PC Board Keying.

## 1.2. MANUAL SET ORGANIZATION

This manual is part of a 5 volume set supporting the iVPI system. The set is organized as follows:

- Volume 1, Installation, Operation, and Theory Manual, includes general overview of the field installation and setup of the iVPI system; including capacity guidelines and allowable board combinations, system operation, and theory of operation.
- Volume 2, Subrack Configuration, describes the subrack configuration including cables and power supplies.
- Volume 3, Vital Subsystem, includes the Vital subsystem board drawings and board reference data.
- Volume 4, Non-Vital Subsystem, is this document. It includes non-vital subsystem board drawings and board reference data.
- Volume 5, Maintenance and Troubleshooting, describes system maintenance and troubleshooting, including discussion of diagnostics and references for the applicable software and hardware manuals.

### 1.3. SUBRACK TERMS

The iVPI System is highly modular in design, implemented in a 19 inch rack mounted card cage (Subrack) with a set of plug-in printed circuit boards (boards) that are applied in varying quantities to meet the needs of specific applications.

The terminology used to define the Subrack and its components is as follows:

- A Subrack is a Chassis with Motherboard
- A System is one or more Subracks filled with the appropriate boards for the application
- When a System is configured with more than one Subrack populated with boards, the individual populated Subracks are Subsystems

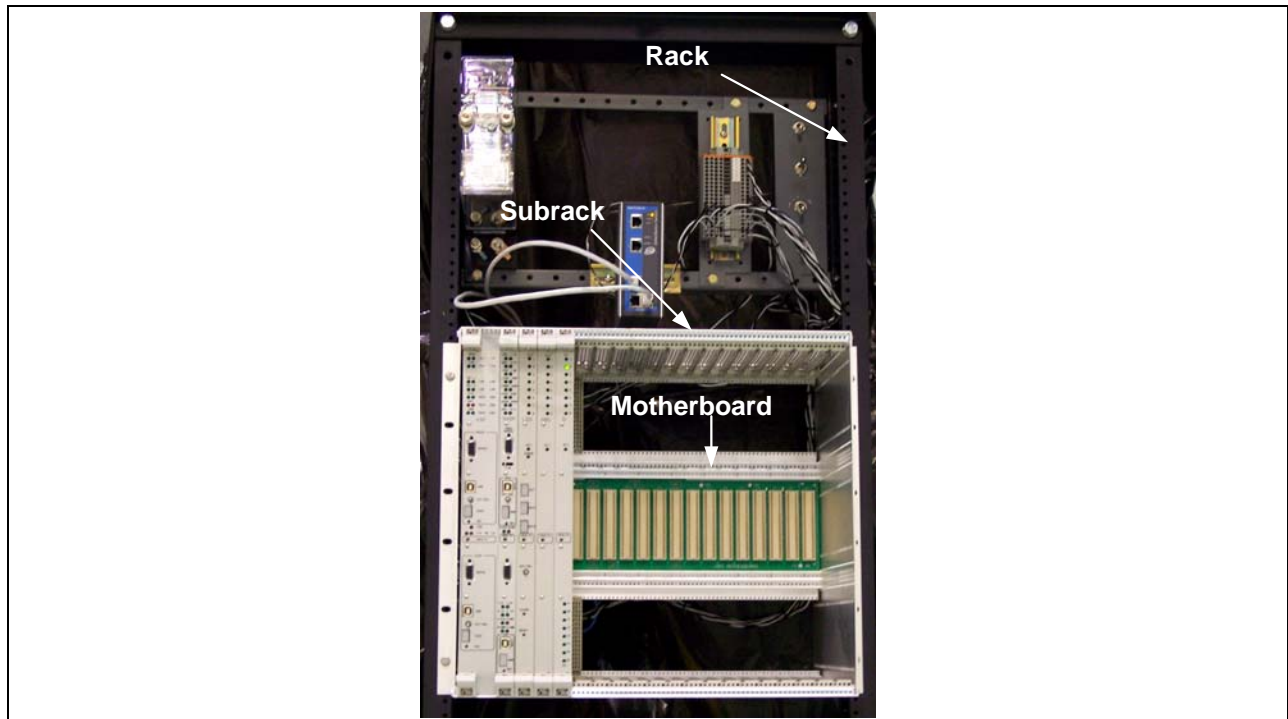


Figure 1–1. iVPI Rack and Subrack

#### 1.4. NON-VITAL SUBSYSTEM

For non-vital applications, the iVPI system consists of one or more Non-Vital System Processor (NVSP) board(s).

The non-vital iVPI system is contained either in a subrack identical to an iVPI Vital system or within a section of a Vital iVPI subrack. Communications between the non-vital system and the Vital system is via the Motherboard (within the subrack when non-vital and Vital systems share the same subrack or an extender cable when the two systems are in different subracks).

The iVPI non-vital system boards are:

- NVSP – Non-Vital System Processor board
- NVI – Non-Vital Input board
- NVO – Non-Vital Output board

In addition to the system boards listed above, the non-vital system may be configured with one or more optional NVSP Interface boards to simplify the physical and electrical connections to the NVSP board:

- NVSP P1 Interface board
- NVSP P3 Interface board

An iVPI System can include up to four NVSP boards on the System Bus, thus allowing many arrangements for load sharing, if required. The NVSP board can also operate in a completely standalone mode independent of being connected via the System Bus to a Vital processor. In either the standalone or in the connected arrangement, each NVSP board can interface with up to 20 non-vital I/O boards (housed in the same Subrack as the NVSP) each with 32 I/O points for a total of 640 non-vital I/O points per NVSP board.

Table 1–1 lists the non-vital printed circuit boards in the order that they are discussed. A board's 10 digit drawing number is also the part number use for ordering the board.

Table 1–1. Non-Vital Printed Circuit Boards Index

Board Type	Drawing Number	Comments
NVSP	31166-428-01	386 Processor, 3 Comm Ports, 2 Ethernet ports, SW 40025-XXX-00
NVI	31166-457-01	32 inputs, 18-33 VDC
NVI	31166-457-02	32 inputs, 9-18 VDC
NVO	31166-458-01	32 Form A mechanical relay outputs, 0-35V AC/DC, 1 A, Power On Reset, Powered from 18-33 VDC
NVO	31166-458-02	32 Form A solid state outputs, 0-35V AC/DC, 1 A, Power On Reset, Powered from 18-33 VDC
NVSP P1 Interface	31166-474-01	2 Ethernet ports
NVSP P3 Interface	31166-475-01	4 Serial ports

**NOTE**

For descriptions of how to troubleshoot the boards using the LEDs and/or Diagnostic displays visible from the board fronts, see Alstom manual P2521B, Volume 5.

Application software is compiled by the tools and downloaded directly to the NVSP via a USB type communication interface.

Figure 1–2 is the block diagram of an example iVPI application using every board type available for the iVPI System. Figure 1–3 is an example iVPI using the expansion system.

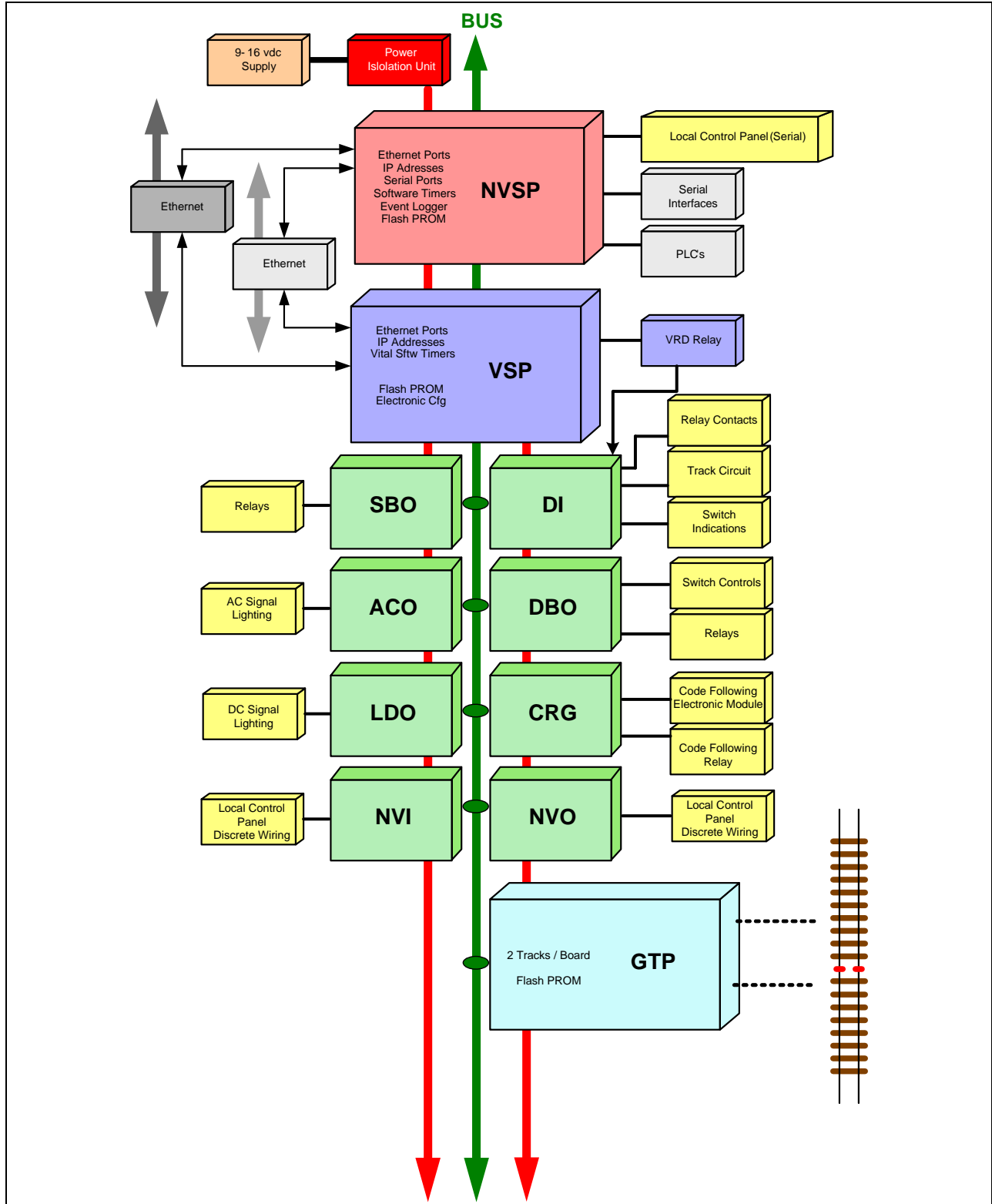


Figure 1–2. Example iVPI Vital / Non-Vital System Application

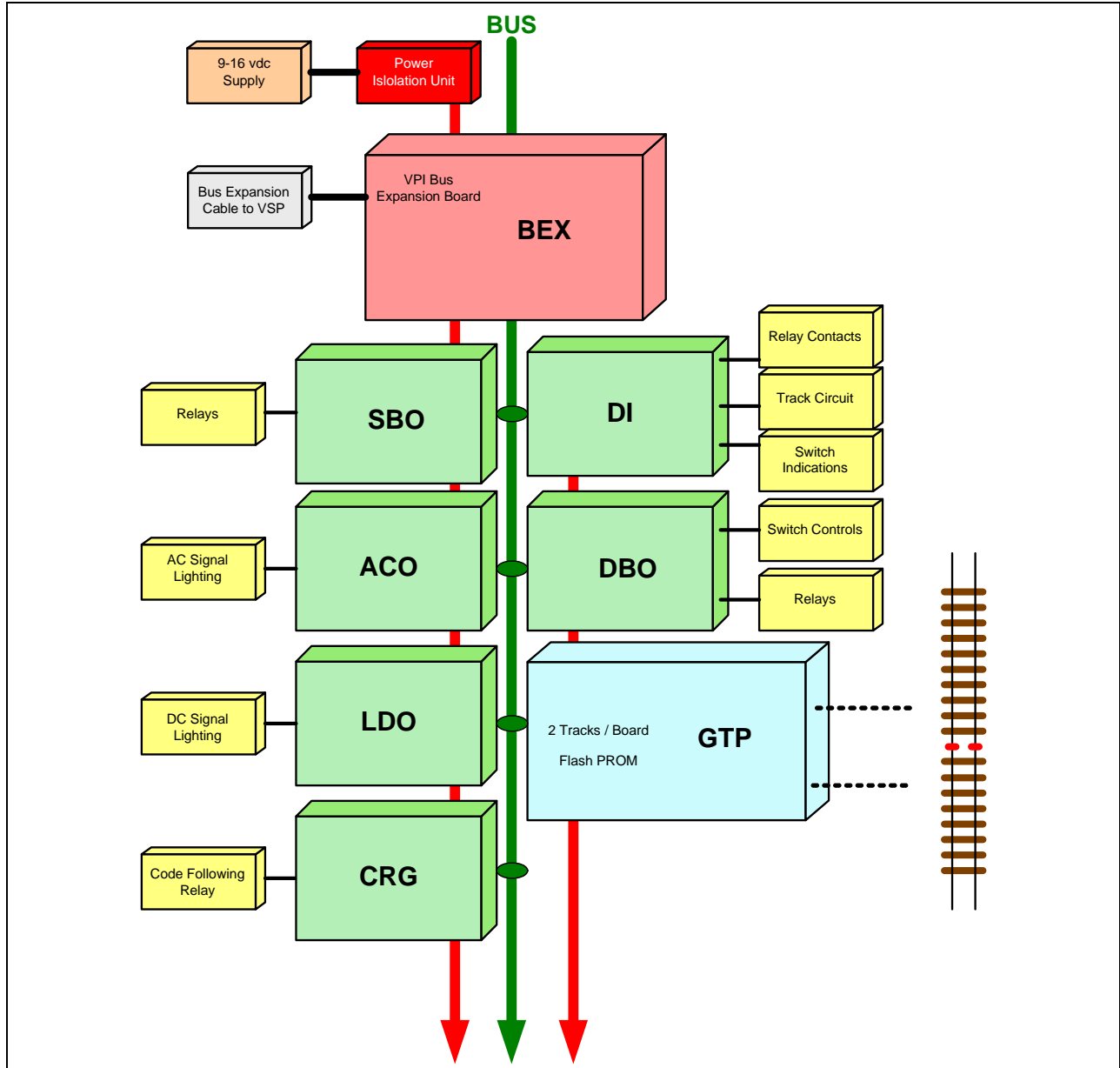


Figure 1-3. Example iVPI Expansion System Application

## 2. SECTION 2 – NVSP (NON-VITAL SYSTEM PROCESSOR) BOARD, P/N 31166-428-XX

### 2.1. GENERAL

This section describes the function of the NVSP board.

### 2.2. INTRODUCTION

The NVSP (Non-Vital System Processor) board is a system board for iVPI as well as a stand-alone non-vital logic processor. It provides the control of the non-vital inputs and outputs for local control of interlockings. It can be used to interface with a communications based Local Control Panel and/or computers.

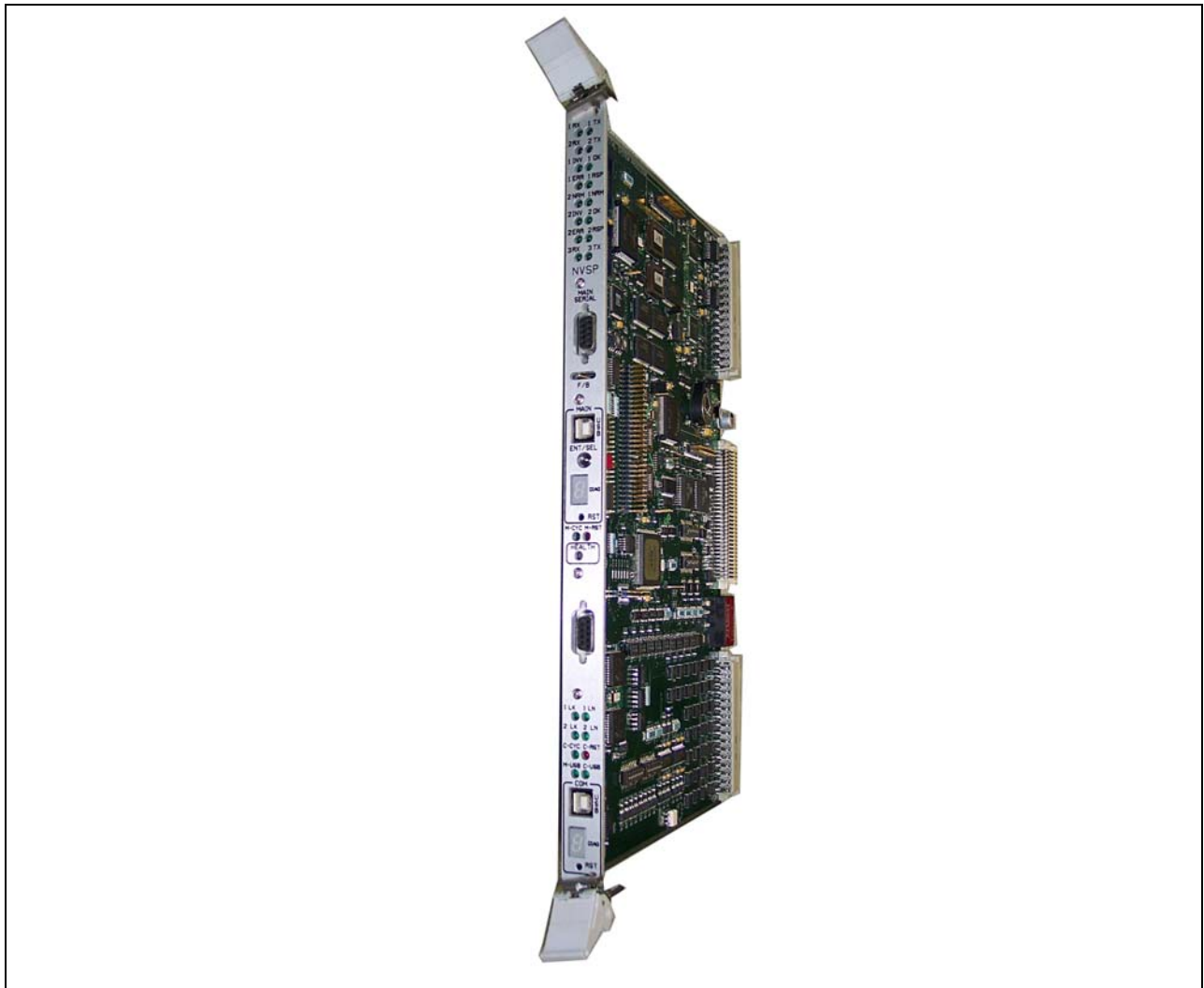


Figure 2–1. NVSP Board

The NVSP can be interfaced directly to standard communication equipment such as Fiber Optic Modems, Multiplexers, and Network Adapters.

The NVSP board can be application programmed with non-vital logic to provide Human Machine Interfaces (HMI), entrance-exit logic and a multitude of other non-vital functions. The NVSP board can be used to interface with communications based Local Control Panel and/or HMI computers; or by using the NVI and NVO boards it can directly interface to discrete wired Local Control Panels and non-vital support functions.

The NVSP board also contains a battery backed-up memory section and clock/calendar to support the onboard DATALOGGER™ software used for logging both Vital and non-vital variables. Three of the communication ports in addition to the two Ethernet ports can be utilized for external non-vital communications. Each port may be configured with the same or with a different communication protocol. The choice of protocols is assigned and configured in the Computer Aided Application tools by the signal engineer.

A library of communication protocols common to the railroad and transit industry is included in the Computer Aided Application package. Typical protocols included are industry standards such as GENISYS, Data Train, MODBUS, and MODBUS/TCP among others.

### 2.2.1. Features

The following is a brief description of NVSP major features:

- Status LEDs indicate Tx/Rx activity for:
  - Serial Ports 1 and 2 support synchronous and asynchronous RS-232, RS-422, and RS-485.
  - Serial Port 3 supports asynchronous RS-422 and RS-485.
  - Serial Port 4, the MAC port, is used for connecting the NVSP Processor to a PC, supports asynchronous RS-232, and is available at the front DB-9 connector or USB port or through P3 on the backplane (switch selectable). A status LED provides the USB connection status.
  - Serial Port 5, of the Communication Processor, is used for connecting to PC, supports asynchronous RS-232, and is available at the front DB-9 connector or a USB port. A status LED provides the USB connection status.
- Two 10/100 base-T Ethernet ports are available through the P1 connector. Control of the network ports is provided by a separate 386EX Communication Processor.
- The Flash ROM may be programmed using a device programmer or through any serial port. Flash ROM programming may be permanently enabled or permanently disabled using programming jumpers on TB10 and TB3 for the NVSP and Communication Processors, respectively.
- Watchdog: The NVSP watchdog function can be enabled/disabled by programming jumper TB5.
- Low Battery indicator is monitored by the power supervisor device via the NVSP Processor. An indication is available as to the valid battery status.
- Real-Time Clock: is battery-backed to keep time when power is removed.
- Board configuration can be specified to the application software through two binary encoded rotary switches.
- Board-Edge Diagnostics: status LED's and two 7-segment displays, one each Main and Communication Processor to indicate various board activities.
- Non-Vital I/O: the NVSP board controls non-vital I/O boards.

### 2.3. INDICATIONS

The NVSP board has LED indications that provide a visual indication of the status of the board, the software, and the communication ports. A Health LED is used to indicate board health status. See Figure 2–2 for an illustration of the board edge, including LEDs, ports, push buttons and 7-segment displays.

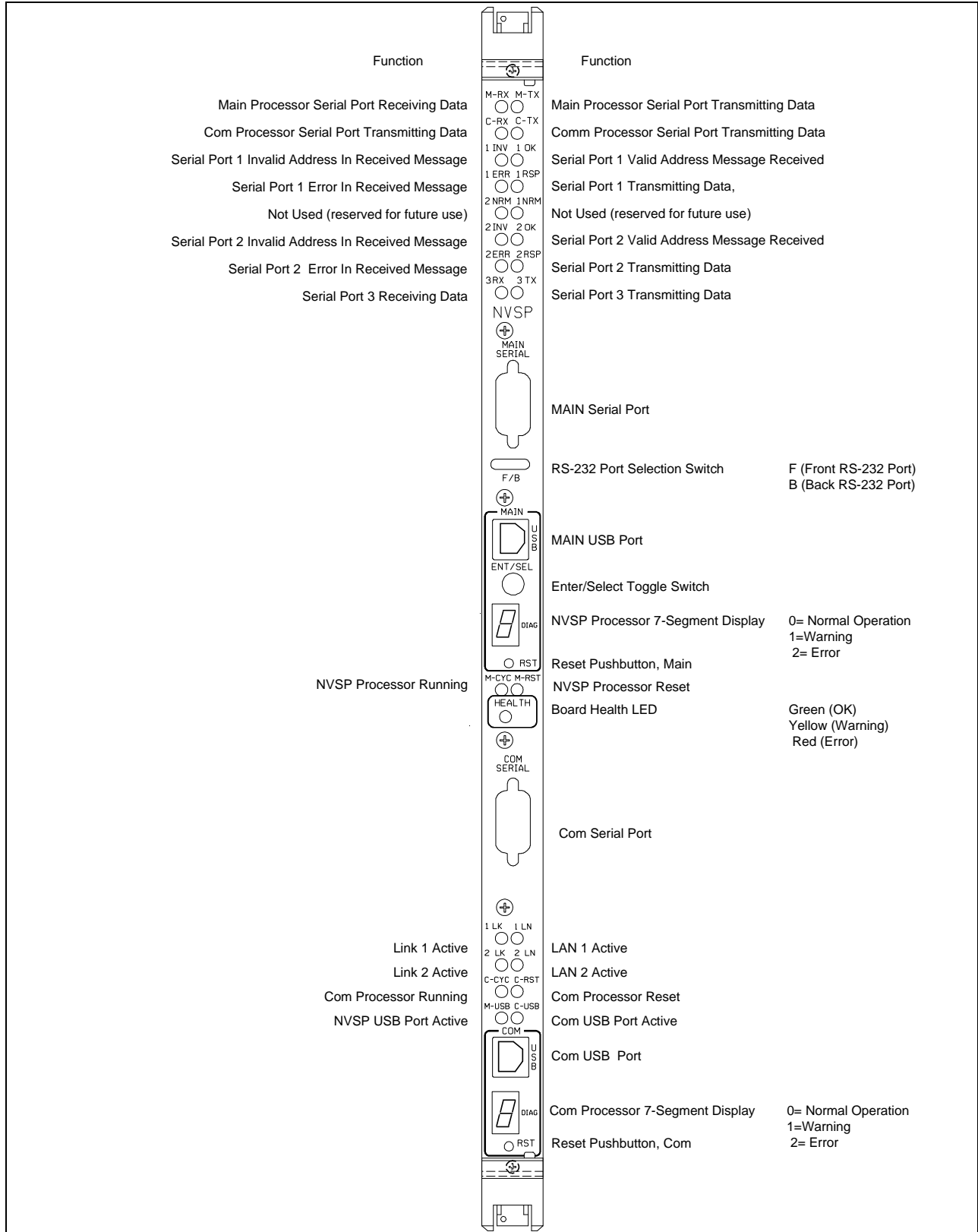


Figure 2–2. NVSP Board Edge

## 2.4. JUMPERS

Table 2–1 shows the jumper assignments for the NVSP Board. All possible functions have a jumper installed even though the jumper may not make an electrical connection. This is done to ensure that there is the correct number of jumpers on the board at all times. See Figure 2–3 for a board layout drawing identifying the NVSP jumper locations and see Figure A–1 for a complete board layout drawing.

Table 2–1. NVSP Board Jumpers

<b>JP1</b>	<b>Function</b>
TB1 (no jumper)	Communication Processor PROMJet Header
TB2 (no jumper)	Communication Processor PROMJet connection points
TB3-1 to TB3-2	Communication Processor Flash PROM write enabled
TB3-2 to TB3-3	Communication Processor Flash PROM write disabled
TB4-1 to TB4-2	Backup battery disconnected (use this position for shipping & storage, also if no battery is installed during operation)
TB4-2 to TB4-3	Backup battery connected
TB5-1 to TB5-2	NVSP Processor watchdog- normal operation
TB5-2 to TB5-3	NVSP Processor watchdog- disable watchdog reset (for emulator use only)
TB6 (no jumper)	NVSP Processor PROMJet Header
TB7 (no jumper)	NVSP Processor PROMJet connection points
TB8 (no jumper)	ASIC Test Header
TB9 (no jumper)	ASIC Programming Header
TB10-1 to TB10-2	NVSP Processor Flash PROM write enabled
TB10-2 to TB10-3	NVSP Processor Flash PROM write disabled



2.5. SERIAL PORTS

A port is assigned RS422/485 or RS232.

Table 2–2. NVSP Board Channel 1 Communication Standard Selection Switch Setting

Standard	SW7 Position
RS422/485	all off
RS232	all on

Table 2–3. NVSP Board Channel 2 Communication Standard Selection Switch Setting

Standard	SW6 Position
RS422/485	all off
RS232	all on

Serial port 4 (the MAC port) uses an EAI-232 transceiver to transmit and receive. An alternative connection for port 4 is via the USB connection J6.

Table 2–4. NVSP Board MAC EIA-232 Port Description

Pin	Function
J3-1	–
J3-2	RXD: receive data
J3-3	TXD: transmit data
J3-4	–
J3-5	COM: isolated common
J3-6	–
J3-7	–
J3-8	–
J3-9	–

Table 2–5. NVSP Board MAC USB Port Description

<b>Pin</b>	<b>Function</b>
J4-1	VBUS
J4-2	D-
J4-3	D+
J4-4	COM
J4-5	Shield
J4-6	Shield

## 2.6. CARD EDGE CONNECTORS

The NVSP Board has three card edge connectors:

- P1, the upper connector, is a 96-pin connector (48 pins populated) used for network connections.
- P2, the middle connector, is a 160-pin connector used to interface with the VSP System Bus, Non-Vital Bus, to supply the NV I/O power, and assign board address.
- P3, the lower connector, is a 96-pin connector (48 pins populated) used for serial port connections.

### **NOTE**

For the user defined inputs and outputs, refer to the .lvc output file generated by the system software CAAPE program.

2.7. SPECIFICATIONS

Table 2–6. NVSP Board Specifications

<b>Specification</b>	<b>31166-428-01</b>
Maximum Number of Boards Per iVPI System	4
Board Slots Required	1
Nominal Voltage	12 VDC
Typical Operating Current	1.25 A
No. of Sync./Async. Ports	2
No. of Async. Only Ports	3
MAC Interface	EIA232
Network Port/Type	Ethernet or Serial

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### **3. SECTION 3 – NVI (NON-VITAL INPUT) BOARD, P/N 31166-457-XX**

#### 3.1. GENERAL

This section describes the Non-Vital Input (NVI) Board used in the iVPI system.

#### 3.2. INTRODUCTION

The Non-Vital Input (NVI) board provides 32 isolated inputs. The input circuits are organized into four groups (1-4) of eight circuits. Each of four groups of eight inputs shares a common signal return. Each input circuit is by default uncommitted and isolated from the logic circuit power common. The input circuit may be configured through jumper headers to act as sinking or sourcing modes. Each input group can be independent connected to unique power sources.

Appropriate transient protection devices are included in the input circuits. A family of NVI boards exists such that they can interface with a customer's unique interface requirements.

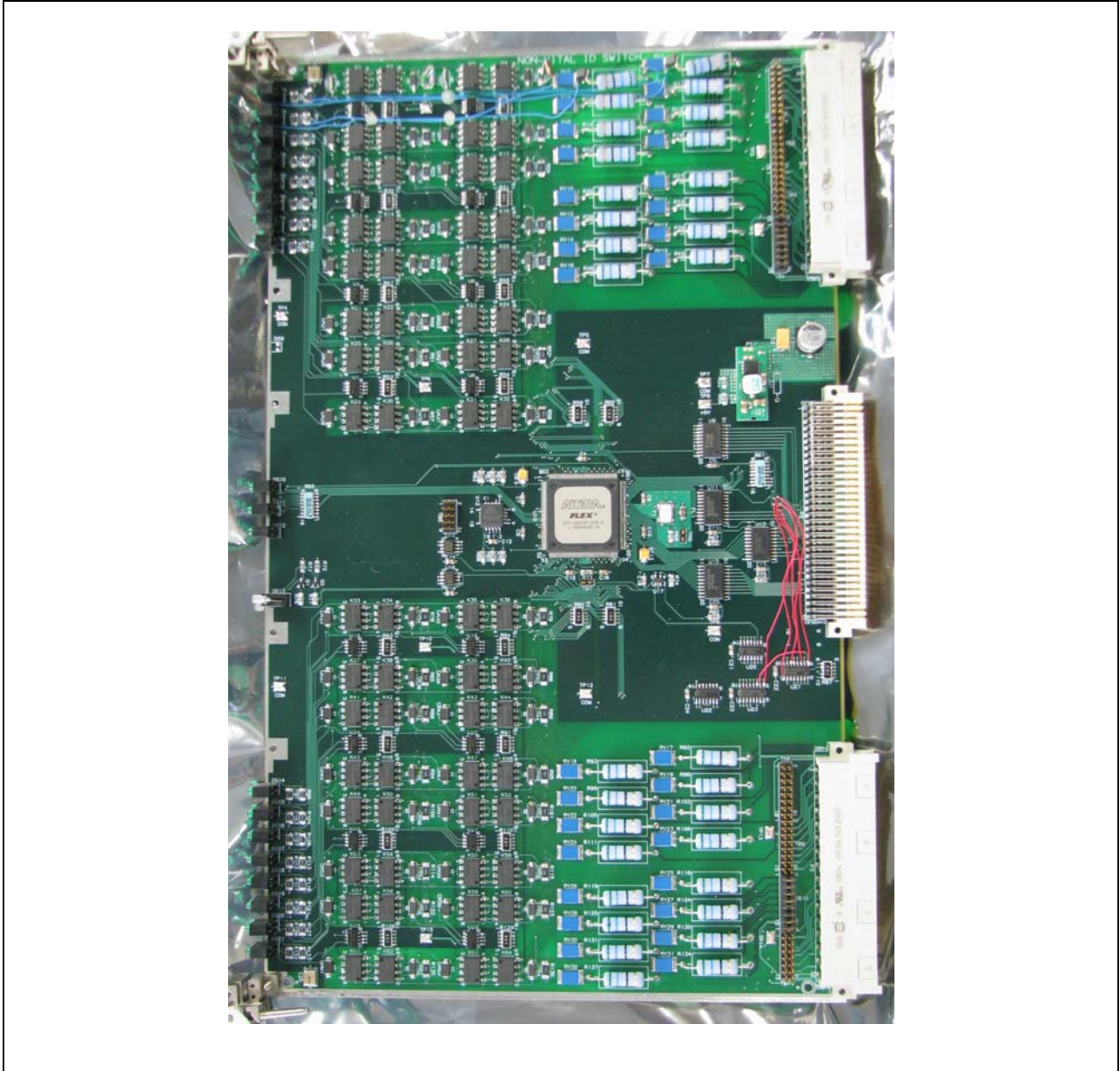


Figure 3–1. NVI Board

### 3.3. INDICATIONS

An LED indication for each input, representing the input state, is found at the board's front edge, see Figure 3–2. A Health LED is used to indicate board health status and board activity.

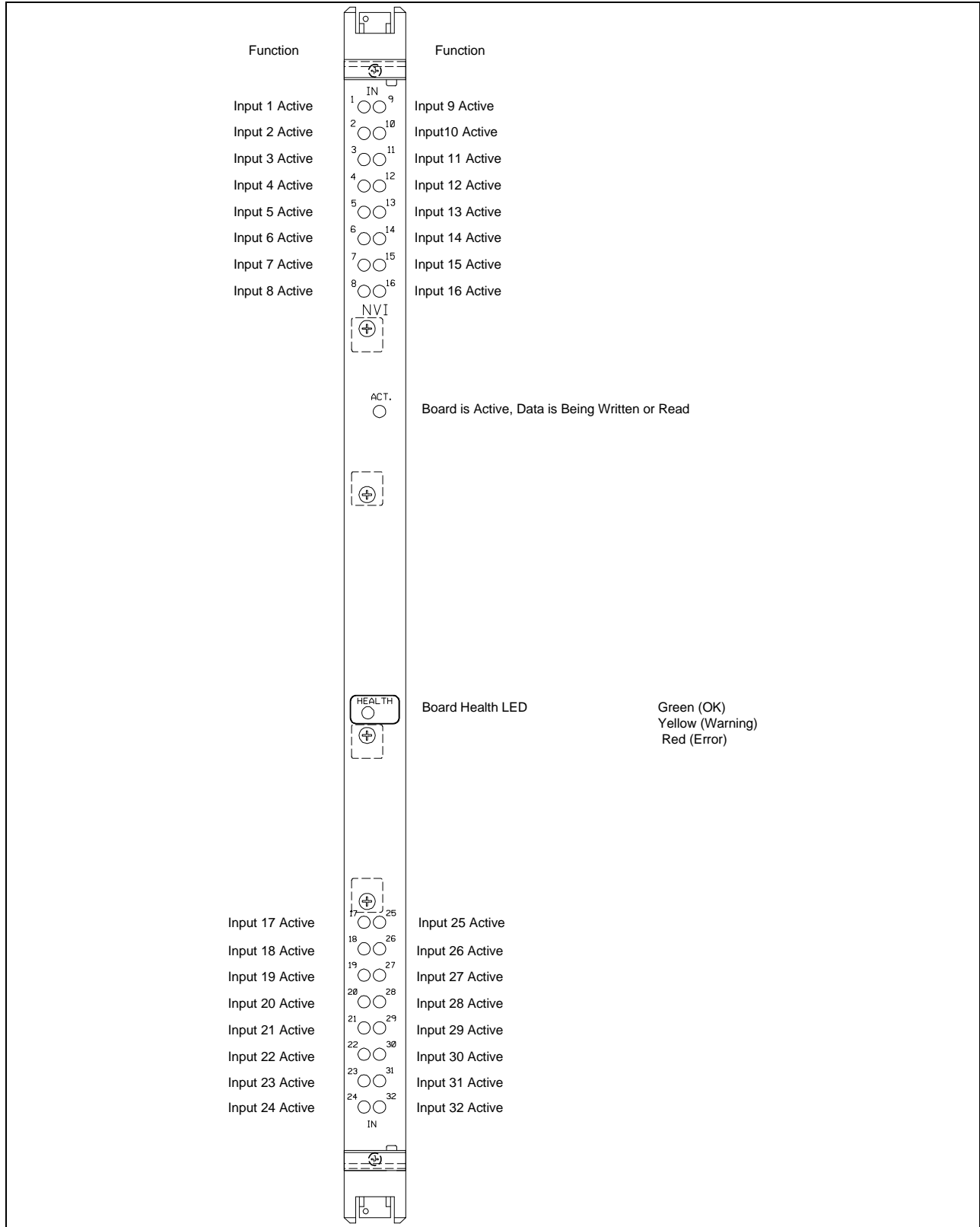


Figure 3–2. NVI Board Edge

### 3.4. CARD EDGE CONNECTORS

NVI Boards have three card edge connectors:

- P1, the top connector, is a 48-pin connector which contains wiring for inputs 1 – 16 and input common connections.
- P2, the middle connector, is a 160-pin connector used for communication with a NVSP board, and also to supply board power.
- P3, the lower connector, is a 48-pin connector which contains wiring for inputs 17 – 32 and input common connections.

The pins on these connectors are not user configurable.

#### **NOTE**

For the user defined inputs and outputs, refer to the .lvc output file generated by the CAAPE program.

Table 3–1. NVI Board P1 Signals

<b>Name</b>	<b>Input Pin +</b>	<b>Input Pin -</b>
Group 2, Input 8	P1-D32	P1-Z32
Group 2, Input 7	P1-D30	P1-Z30
Group 2, Input 6	P1-D28	P1-Z28
Group 2, Input 5	P1-D26	P1-Z26
Group 2, Input 4	P1-D24	P1-Z24
Group 2, Input 3	P1-D22	P1-Z22
Group 2, Input 2	P1-D20	P1-Z20
Group 2, Input 1	P1-D18	P1-Z18
Group 1, Input 8	P1-D16	P1-Z16
Group 1, Input 7	P1-D14	P1-Z14
Group 1, Input 6	P1-D12	P1-Z12
Group 1, Input 5	P1-D10	P1-Z10
Group 1, Input 4	P1-D8	P1-Z8
Group 1, Input 3	P1-D6	P1-Z6
Group 1, Input 2	P1-D4	P1-Z4
Group 1, Input 1	P1-D2	P1-Z2
Group 1, Power In	P1-B2	P1-B4
Group 2, Power In	P1-B30	P1-B32

Table 3–2. NVI Board P3 Signals

<b>Name</b>	<b>Input Pin +</b>	<b>Input Pin -</b>
Group 4, Input 8	P3-D32	P3-Z32
Group 4, Input 7	P3-D30	P3-Z30
Group 4, Input 6	P3-D28	P3-Z28
Group 4, Input 5	P3-D26	P3-Z26
Group 4, Input 4	P3-D24	P3-Z24
Group 4, Input 3	P3-D22	P3-Z22
Group 4, Input 2	P3-D20	P3-Z20
Group 4, Input 1	P3-D18	P3-Z18
Group 3, Input 8	P3-D16	P3-Z16
Group 3, Input 7	P3-D14	P3-Z14
Group 3, Input 6	P3-D12	P3-Z12
Group 3, Input 5	P3-D10	P3-Z10
Group 3, Input 4	P3-D8	P3-Z8
Group 3, Input 3	P3-D6	P3-Z6
Group 3, Input 2	P3-D4	P3-Z4
Group 3, Input 1	P3-D2	P3-Z2
Group 3, Power In	P3-B2	P3-B4
Group 4, Power In	P3-B30	P3-B32

### 3.5. USER SETTINGS

The following table describes the user/field setting on this board. See Figure 3–3 for a board layout drawing identifying these NVI jumper locations and see Figure A–2 for a complete board layout drawing.

Table 3–3. NVI Board Sourcing Jumper Selection

<b>Sourcing Selection (Group N Power)</b>	<b>Sinking Selection (Group N Common)</b>	<b>Affected Input</b>
TB1: 1-2	TB2: 1-2	Group 1 Input 1
TB1: 3-4	TB2: 3-4	Group 1 Input 2
TB1: 5-6	TB2: 5-6	Group 1 Input 3
TB1: 7-8	TB2: 7-8	Group 1 Input 4
TB1: 9-10	TB2: 9-10	Group 1 Input 5
TB1: 11-12	TB2: 11-12	Group 1 Input 6
TB1: 13-14	TB2: 13-14	Group 1 Input 7
TB1: 15-16	TB2: 15-16	Group 1 Input 8
TB3: 1-2	TB4: 1-2	Group 2 Input 1
TB3: 3-4	TB4: 3-4	Group 2 Input 2
TB3: 5-6	TB4: 5-6	Group 2 Input 3
TB3: 7-8	TB4: 7-8	Group 2 Input 4
TB3: 9-10	TB4: 9-10	Group 2 Input 5
TB3: 11-12	TB4: 11-12	Group 2 Input 6
TB3: 13-14	TB4: 13-14	Group 2 Input 7
TB3: 15-16	TB4: 15-16	Group 2 Input 8
TB8: 1-2	TB9: 1-2	Group 3 Input 1
TB8: 3-4	TB9: 3-4	Group 3 Input 2
TB8: 5-6	TB9: 5-6	Group 3 Input 3
TB8: 7-8	TB9: 7-8	Group 3 Input 4
TB8: 9-10	TB9: 9-10	Group 3 Input 5
TB8: 11-12	TB9: 11-12	Group 3 Input 6
TB8: 13-14	TB9: 13-14	Group 3 Input 7
TB8: 15-16	TB9: 15-16	Group 3 Input 8
TB10: 1-2	TB11: 1-2	Group 4 Input 1

Jumpered = Group Source Input

Table 3–2. NVI Board Sourcing Jumper Selection (Cont.)

<b>Sourcing Selection (Group N Power)</b>	<b>Sinking Selection (Group N Common)</b>	<b>Affected Input</b>
TB10: 3-4	TB11: 3-4	Group 4 Input 2
TB10: 5-6	TB11: 5-6	Group 4 Input 3
TB10: 7-8	TB11: 7-8	Group 4 Input 4
TB10: 9-10	TB11: 9-10	Group 4 Input 5
TB10: 11-12	TB11: 11-12	Group 4 Input 6
TB10: 13-14	TB11: 13-14	Group 4 Input 7
TB10: 15-16	TB11: 15-16	Group 4 Input 8

Jumpered = Group Source Input

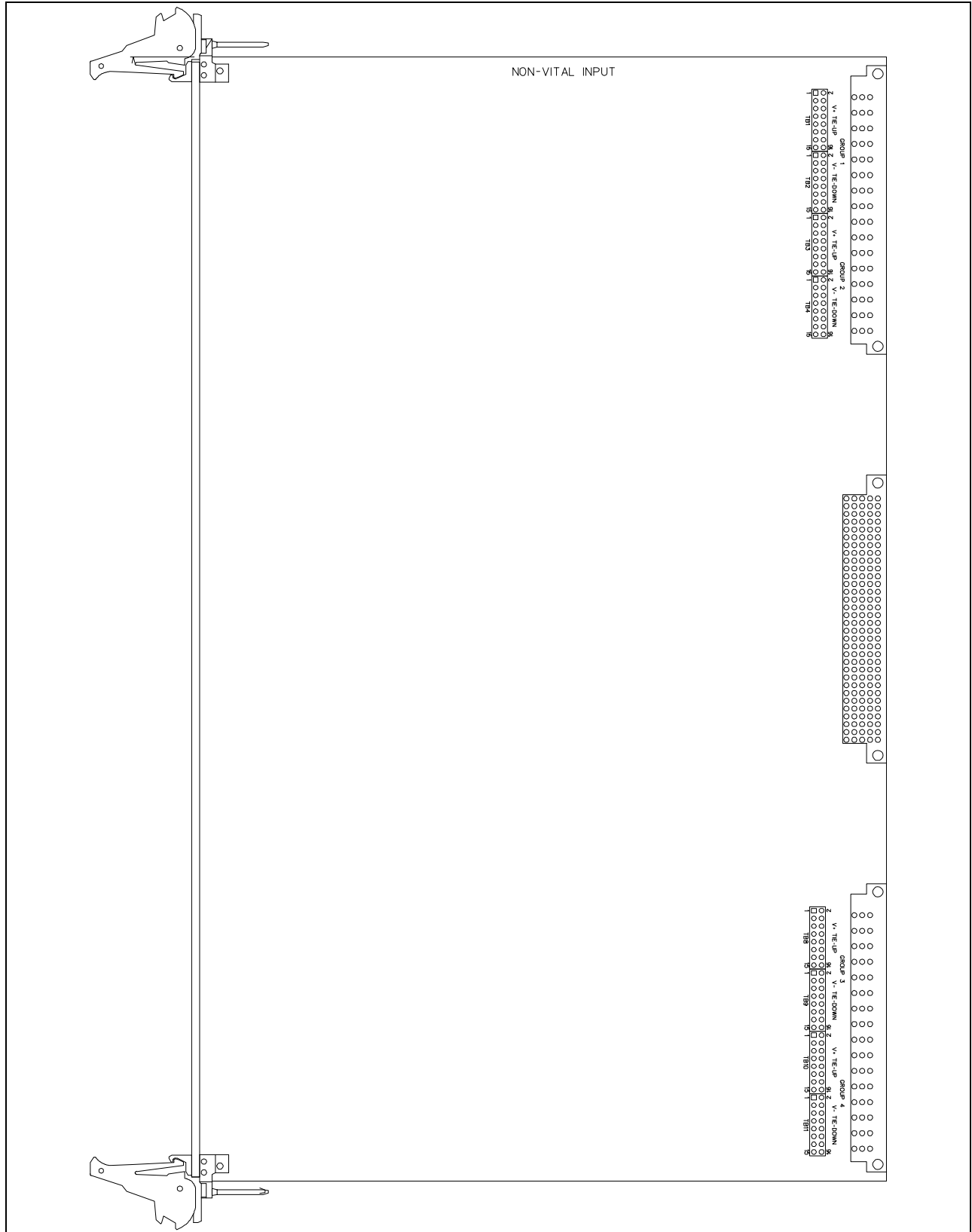


Figure 3-3. NVI Board Jumper Locations

3.6. SPECIFICATIONS/ASSEMBLY DIFFERENCES

Table 3–4. NVI Board Specifications/Assembly Differences

Specification	31166-457	
	-01	-02
Maximum Number of Boards Per iVPI Main System Rack	19	
Maximum Number of Boards Per iVPI Expansion Rack	20	
Board Slots Required	1	
Number of Ports Per Board	32	
Maximum Board Logic Current	83 mA	
Minimum Input Voltage Per Port	18.0 VDC	9.0 VDC
Maximum Input Voltage Per Port	36.0 VDC	18.0 VDC
Minimum Activation Current Per Port	7 mA (Source)	

## **4. SECTION 4 – NVO (NON-VITAL OUTPUT) BOARD, P/N 31166-458-XX**

### **4.1. GENERAL**

This section describes the Non-Vital Output (NVO) Board used in the iVPI system.

### **4.2. INTRODUCTION**

Non-Vital Output (NVO) boards provide 32 isolated outputs controlled by the NVSP board. Two version of the board are available: a mechanical relay output version (form-A and form-C) and a solid state version (form-A only). For both board types, the output circuits are organized into four groups (1-4) of eight circuits. The mechanical relay output version is capable of providing 16 form-A switches and 16 form-C switches. The solid-state output version is capable of providing 32 form-A switches.

Appropriate transient protection devices are included in the output circuits. A family of NVO boards exists such that they can interface with a customer's unique interface requirements.

When removing or inserting a NVO Board for test or maintenance purposes, follow these important instructions:

1. The power supply for this board and for the non-vital processor board (NVSP) must be off.
2. The external power supplies for relays and outputs to this board must also be off.

This is important because:

- It helps to avoid damage to both the NVO and other boards.
- It assures an orderly power-up sequence that avoids unwanted output states.

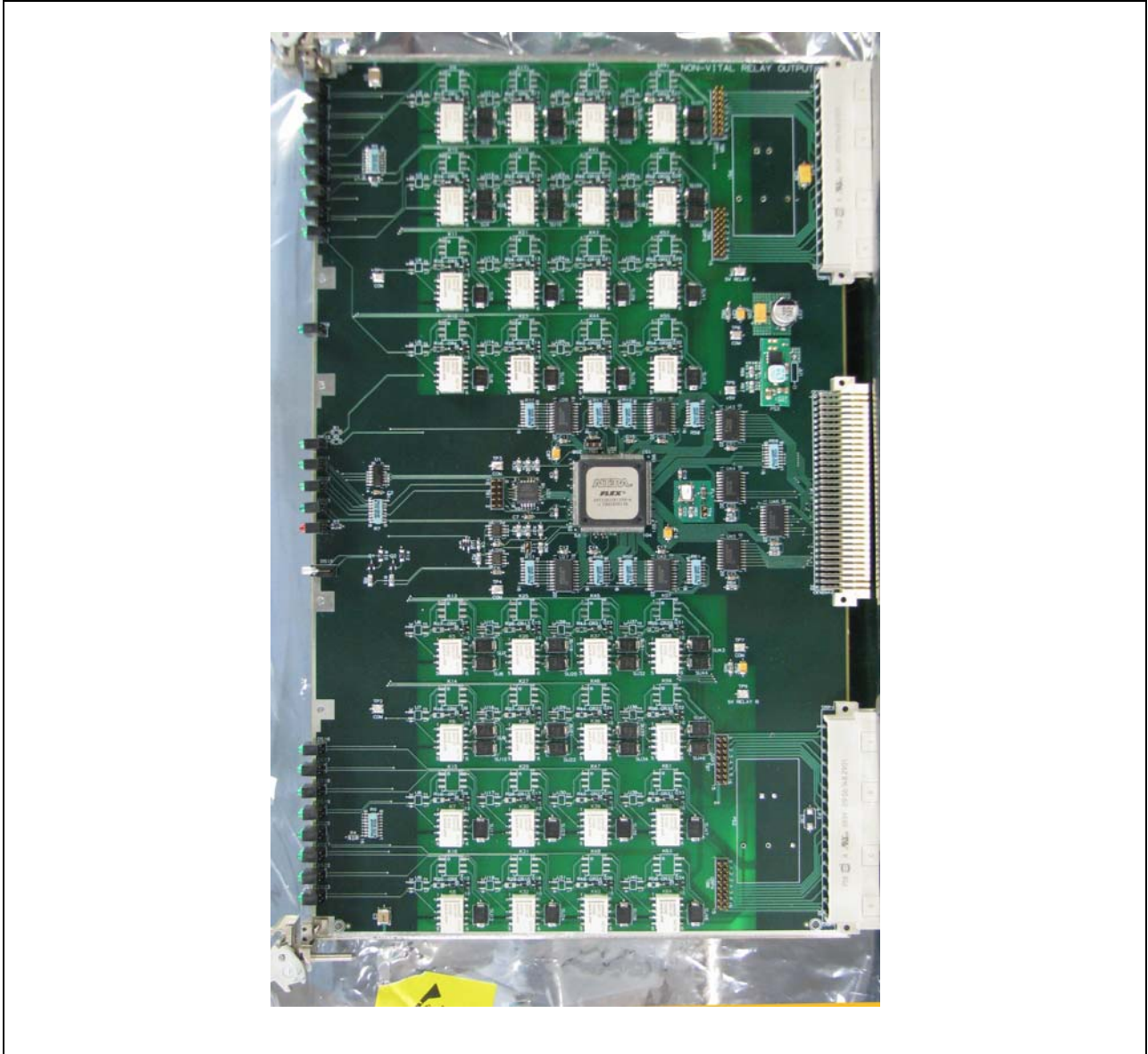


Figure 4-1. NVO Board

#### 4.2.1. Isolated Outputs

Two isolated power feeds for the output circuits separate the power for the field circuitry. There are two separate power feeds. Groups 1 and 2 have one power feed, while groups 3 and 4 have another power feed. The outputs are grouped in four groups with 8 outputs each. The outputs on the P1 and P3 connectors are assigned two pins each. When the output is activated, these two pins are electrically closed (i.e. connected), allowing current flow.

Secondary transient protection in the form of a suppressor is included across the output contacts. These suppressors afford protection against induced transients. Be aware that these outputs are not vitally isolated.

#### **NOTE**

The isolation is provided to allow versatility in system application and a degree of noise elimination. The isolation is NOT VITAL. Any field supply used for Vital functions CANNOT be used with this board.

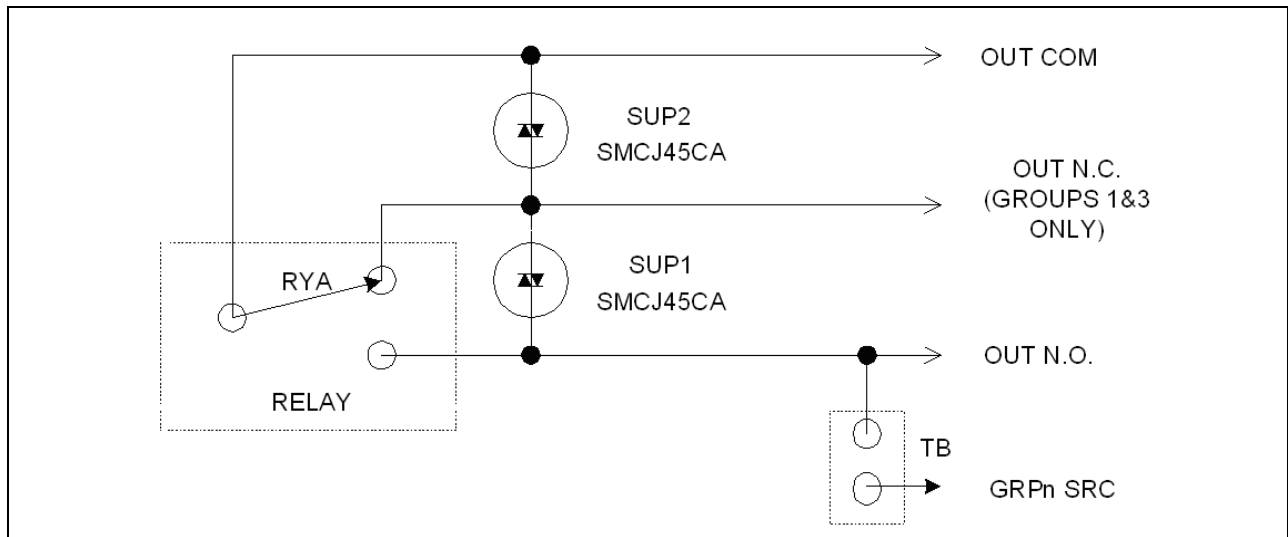


Figure 4–2. Typical Mechanical Relay Output Arrangement

### 4.3. INDICATIONS

An LED indication for each output, representing the output state, is found at the board's front edge, see Figure 4–3. A Health LED is used to indicate board health status and board activity.

In addition, several status LEDs indicate active NVSP access to the board.

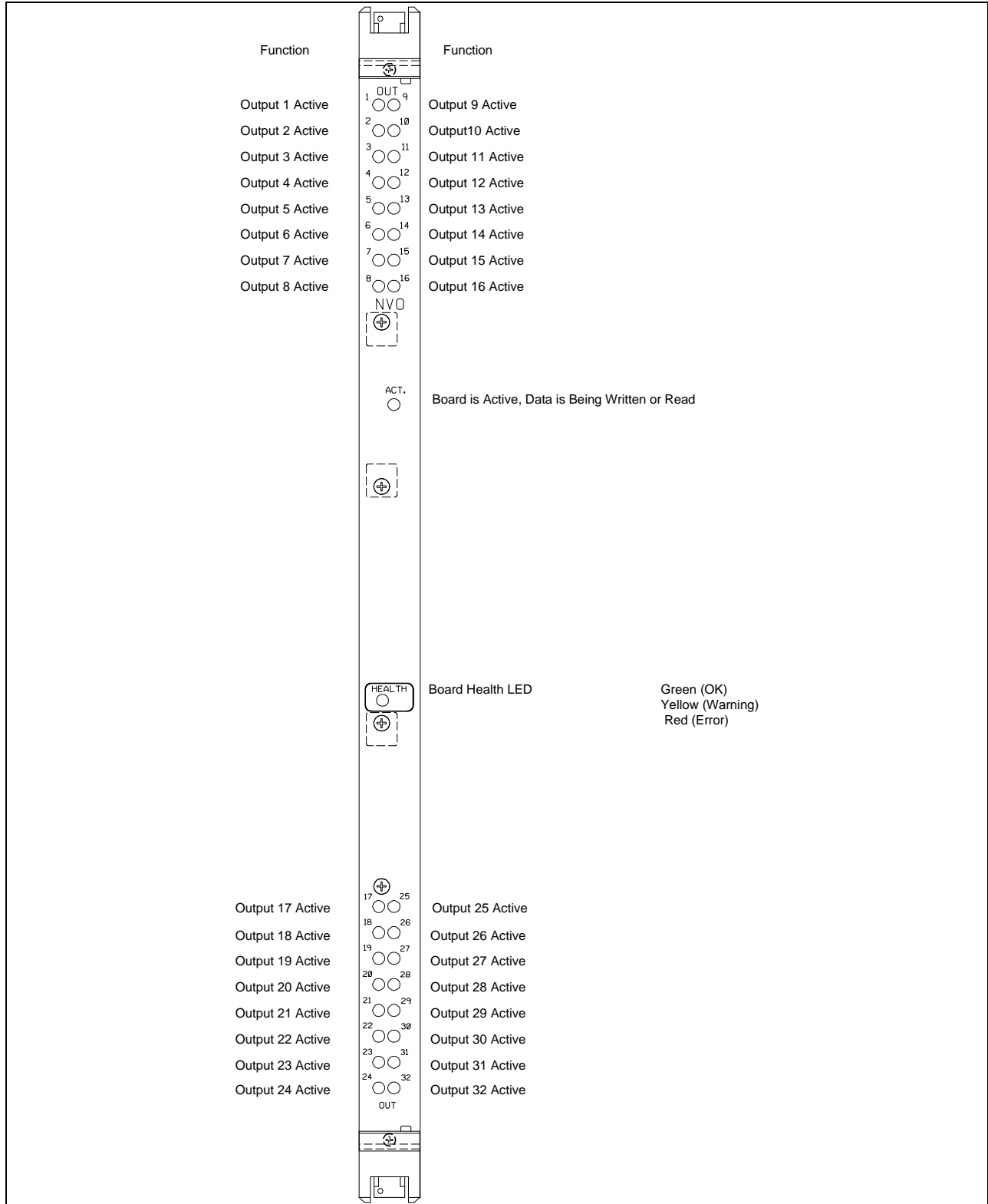


Figure 4–3. NVO Board Edge

#### 4.4. CARD EDGE CONNECTORS

The NVO Board has three card edge connectors:

- P1, the top connector, is a 36-pin connector which contains wiring for outputs 1 – 16 and power supply connections.
- P2, the middle connector, is a 160-pin connector used to interface with the NVSP Non-Vital Bus, power, and I<sup>2</sup>C Bus.
- P3, the lower connector, is a 36-pin connector which contains wiring for outputs 17 – 32 and power supply connections.

The pins on these connectors are not user configurable.

Table 4–1. NVO Board Output Terminals

Output	Heal	Back*	Front	Output	Heal	Back*	Front
1	P1-Z2	P1-B2	P1-D2	17	P3-Z2	P3-B2	P3-D2
2	P1-Z4	P1-B4	P1-D4	18	P3-Z4	P3-B4	P3-D4
3	P1-Z6	P1-B6	P1-D6	19	P3-Z6	P3-B6	P3-D6
4	P1-Z8	P1-B8	P1-D8	20	P3-Z8	P3-B8	P3-D8
5	P1-Z10	P1-B10	P1-D10	21	P3-Z10	P3-B10	P3-D10
6	P1-Z12	P1-B12	P1-D12	22	P3-Z12	P3-B12	P3-D12
7	P1-Z14	P1-B14	P1-D14	23	P3-Z14	P3-B14	P3-D14
8	P1-Z16	P1-B16	P1-D16	24	P3-Z16	P3-B16	P3-D16
9	P1-Z18	N/C	P1-D18	25	P3-Z18	N/C	P3-D18
10	P1-Z20	N/C	P1-D20	26	P3-Z20	N/C	P3-D20
11	P1-Z22	N/C	P1-D22	27	P3-Z22	N/C	P3-D22
12	P1-Z24	N/C	P1-D24	28	P3-Z24	N/C	P3-D24
13	P1-Z26	N/C	P1-D26	29	P3-Z26	N/C	P3-D26
14	P1-Z28	N/C	P1-D28	30	P3-Z28	N/C	P3-D28
15	P1-Z30	N/C	P1-D30	31	P3-Z30	N/C	P3-D30
16	P1-Z32	N/C	P1-D32	32	P3-Z32	N/C	P3-D32

\*the Back connection is only available for the Mechanical Relay version of the board  
 N/C = No Connection

**NOTE**

For the user defined inputs and outputs, refer to the .lvc output file generated by the CAAPE program.

#### 4.5. USER SETTINGS

The following table describes the user/field setting on this board. See Figure 4–4 for a board layout drawing identifying these NVO jumper locations and see Figure A–3 for a complete board layout drawing.

Table 4–2. NVO Board Sourcing Jumper Selection

<b>Group</b>	<b>Terminal Selection</b>	<b>Sourcing Output</b>
GR1	TB5: 1-2	Group 1 Output 1
	TB5: 3-4	Group 1 Output 2
	TB5: 5-6	Group 1 Output 3
	TB5: 7-8	Group 1 Output 4
	TB5: 9-10	Group 1 Output 5
	TB5: 11-12	Group 1 Output 6
	TB5: 13-14	Group 1 Output 7
	TB5: 1: 15-16	Group 1 Output 8
GR2	TB6: 1-2	Group 2 Output 1
	TB6: 3-4	Group 2 Output 2
	TB6: 5-6	Group 2 Output 3
	TB6: 7-8	Group 2 Output 4
	TB6: 9-10	Group 2 Output 5
	TB6: 11-12	Group 2 Output 6
	TB6: 13-14	Group 2 Output 7
	TB6: 15-16	Group 2 Output 8
GR3	TB7: 1-2	Group 3 Output 1
	TB7: 3-4	Group 3 Output 2
	TB7: 5-6	Group 3 Output 3
	TB7: 7-8	Group 3 Output 4
	TB7: 9-10	Group 3 Output 5
	TB7: 11-12	Group 3 Output 6
	TB7: 13-14	Group 3 Output 7
	TB7: 15-16	Group 3 Output 8

Jumpered = Source Output

Table 4–2. NVO Board Sourcing Jumper Selection (Cont.)

<b>Group</b>	<b>Terminal Selection</b>	<b>Sourcing Output</b>
GR4	TB8: 1-2	Group 4 Output 1
	TB8: 3-4	Group 4 Output 2
	TB8: 5-6	Group 4 Output 3
	TB8: 7-8	Group 4 Output 4
	TB8: 9-10	Group 4 Output 5
	TB8: 11-12	Group 4 Output 6
	TB8: 13-14	Group 4 Output 7
	TB8: 15-16	Group 4 Output 8

Jumpered = Source Output

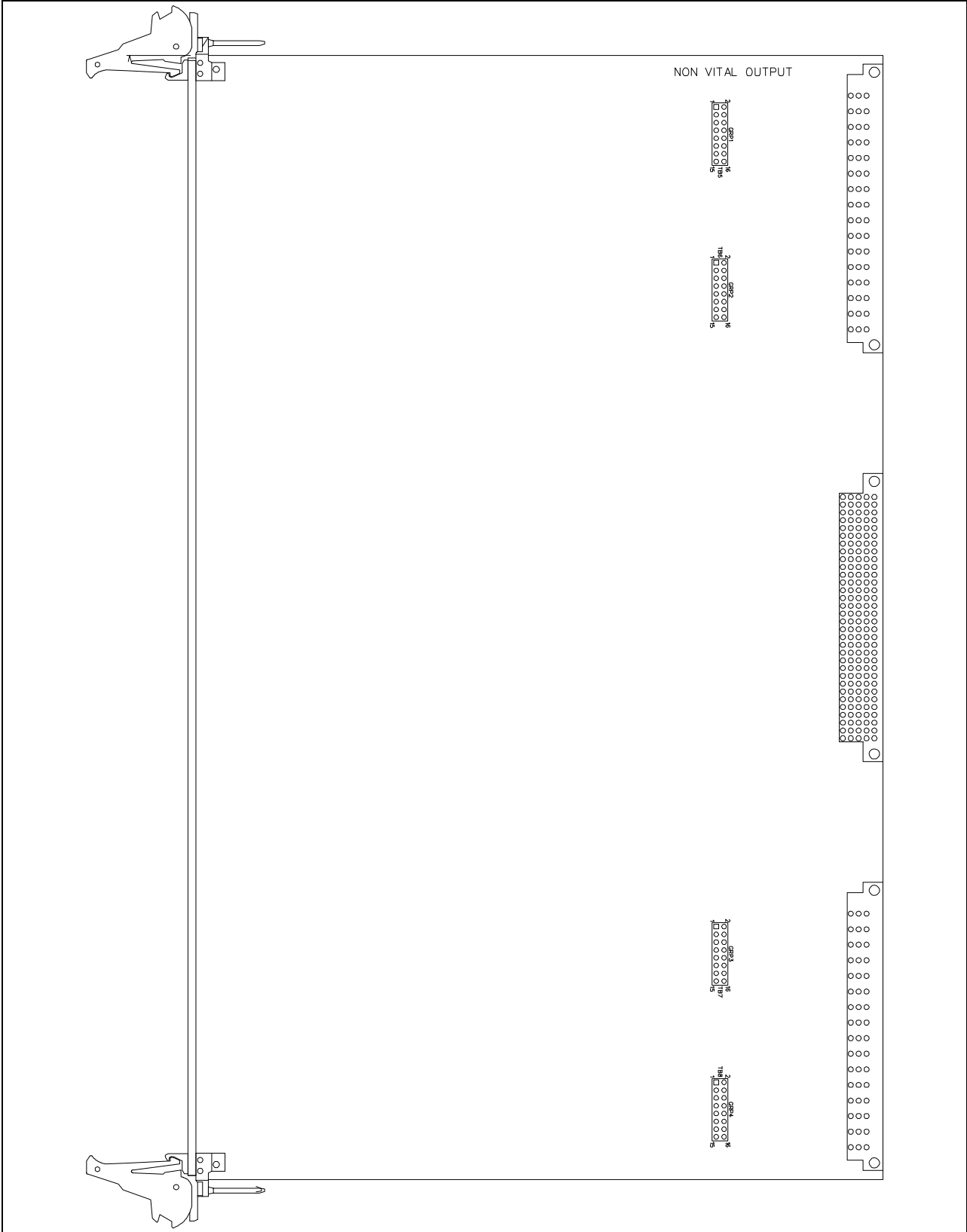


Figure 4-4. NVO Board Jumper Locations

4.6. SPECIFICATIONS/ASSEMBLY DIFFERENCES

Table 4–3. NVO Board Specifications/Assembly Differences

Specification	31166-458	
	-01	-02
Maximum Number of Boards Per NVSP Subsystem	18	
Board Slots Required	1	
Number of Ports Per Board	32	
Maximum Board Logic Current	208 mA	
Minimum Output Supply Voltage	9.0 VDC	
Maximum Output Supply Voltage	18.0 VDC	
Maximum Voltage Per Output Port	35 VDC 24 VAC RMS	
Maximum Current per Relay Contact Port	0.5 A	NA
Maximum Current per Solid State Relay Port	NA	0.5 A

## 5. NVSP INTERFACE BOARDS, P/N 31166-474-XX, 31166-475-XX

### 5.1. GENERAL

This Section describes the NVSP Interface boards. See Figures A–4 and A–5 for board layout drawings.

### 5.2. INTRODUCTION

An iVPI may be configured to use two NVSP Interface boards to provide additional connectivity to the NVSP board:

- NVSP P1 Interface Board
- NVSP P3 Interface Board

### 5.3. NVSP P1 INTERFACE BOARD OPERATION

The NVSP P1 Interface board (P/N 31166-474-01) is located at P1 on the NVSP board to provide additional connectivity to the NVSP board:

- Two RJ45 modular jacks connect to the NVSP board's Ethernet Ports

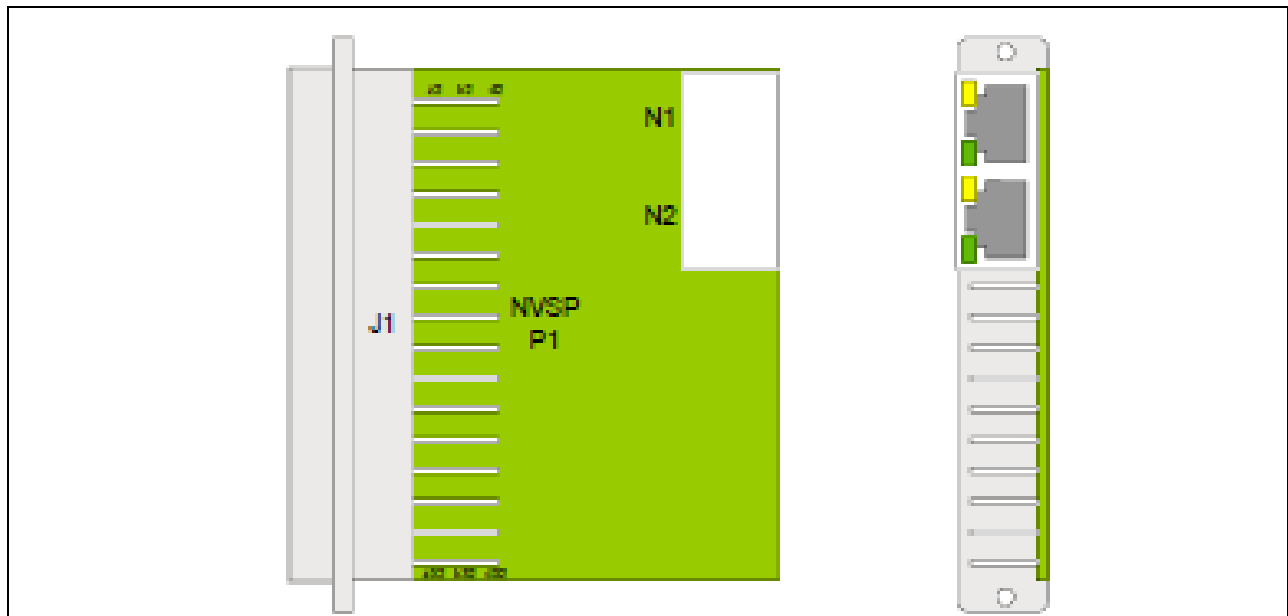


Figure 5–1. NVSP P1 Interface Board

#### 5.4. NVSP P3 INTERFACE BOARD OPERATION

The NVSP P3 Interface board (P/N 31166-475-01) is located at P3 on the NVSP board to provide additional connectivity to the VSP board:

- Two EIA RS-232 DB-25 connectors that shall to the NVSP board's serial ports 1 and 2:
  - One connector is labeled Port 1
  - One connector is labeled Port 2
- One RJ45 modular jack connect to the NVSP board's MAC Port
- One RJ45 modular jack connect to the NVSP board's serial port 3, labeled Port 3
- One RJ12 modular jack for use with the NVSP board's Health Status

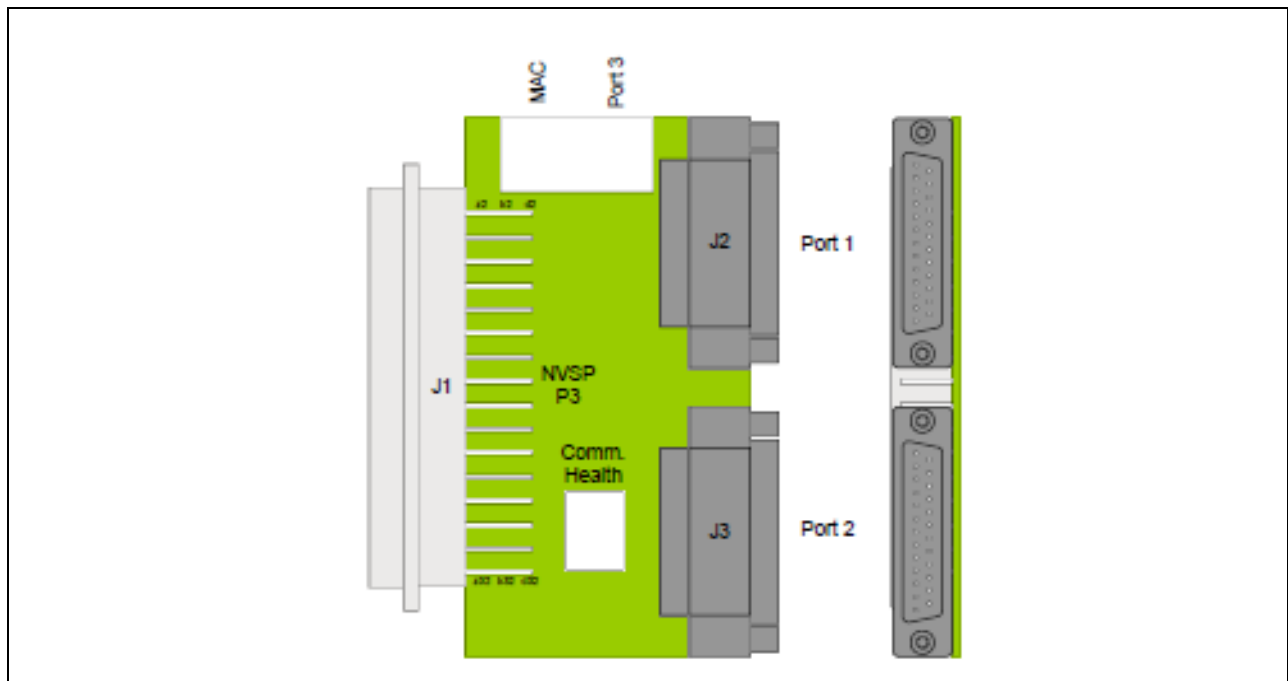


Figure 5–2. NVSP P3 Interface Board

## **A. APPENDIX A – NON-VITAL BOARD LAYOUT DRAWINGS**

### **A.1. GENERAL**

This appendix contains layout drawings of the boards discussed in this manual.

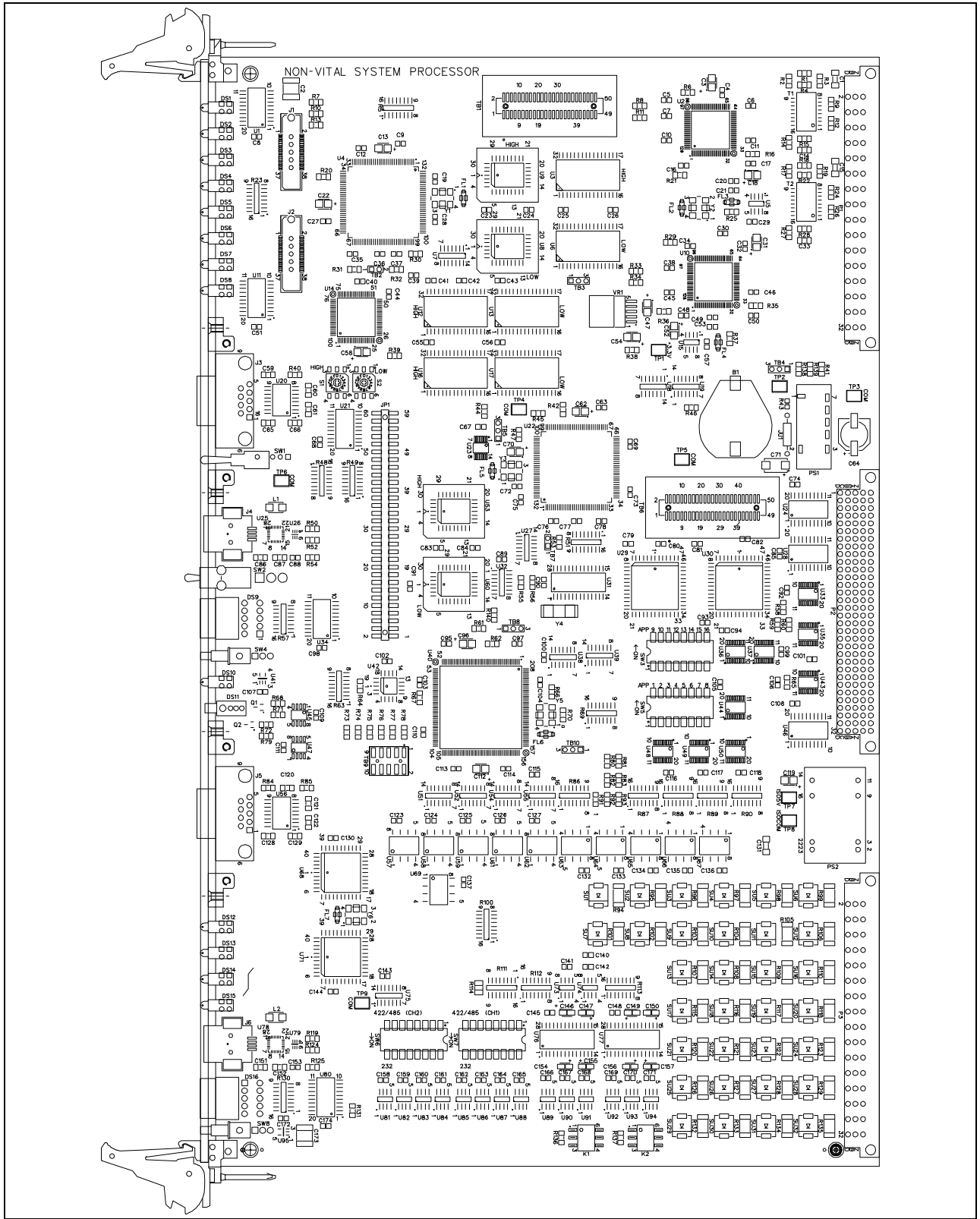


Figure A-1. NVSP Board, P/N 31166-428-01

Non-Vital Board Layout Drawings

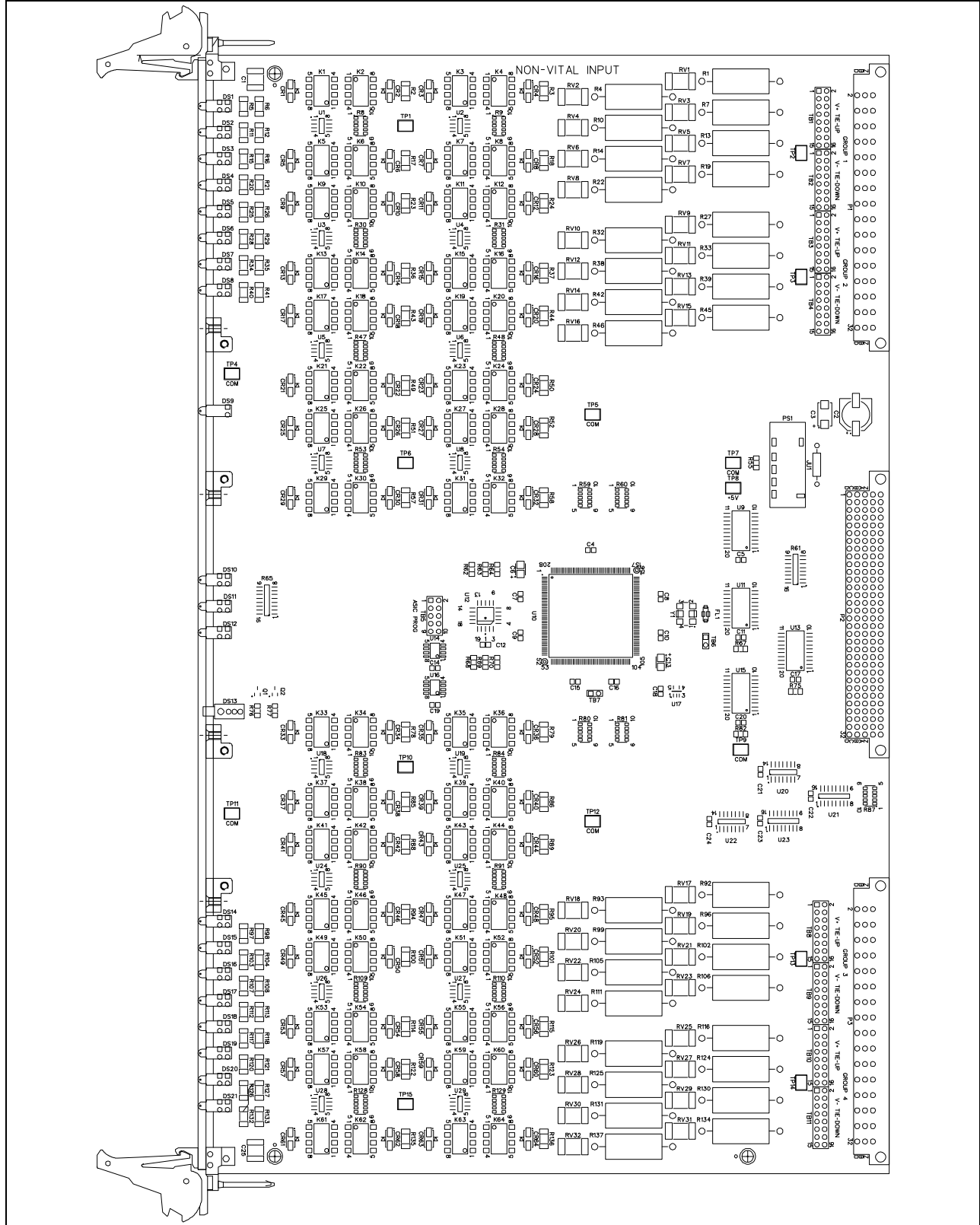


Figure A-2. NVI Board, P/N 31166-457-01 and -02

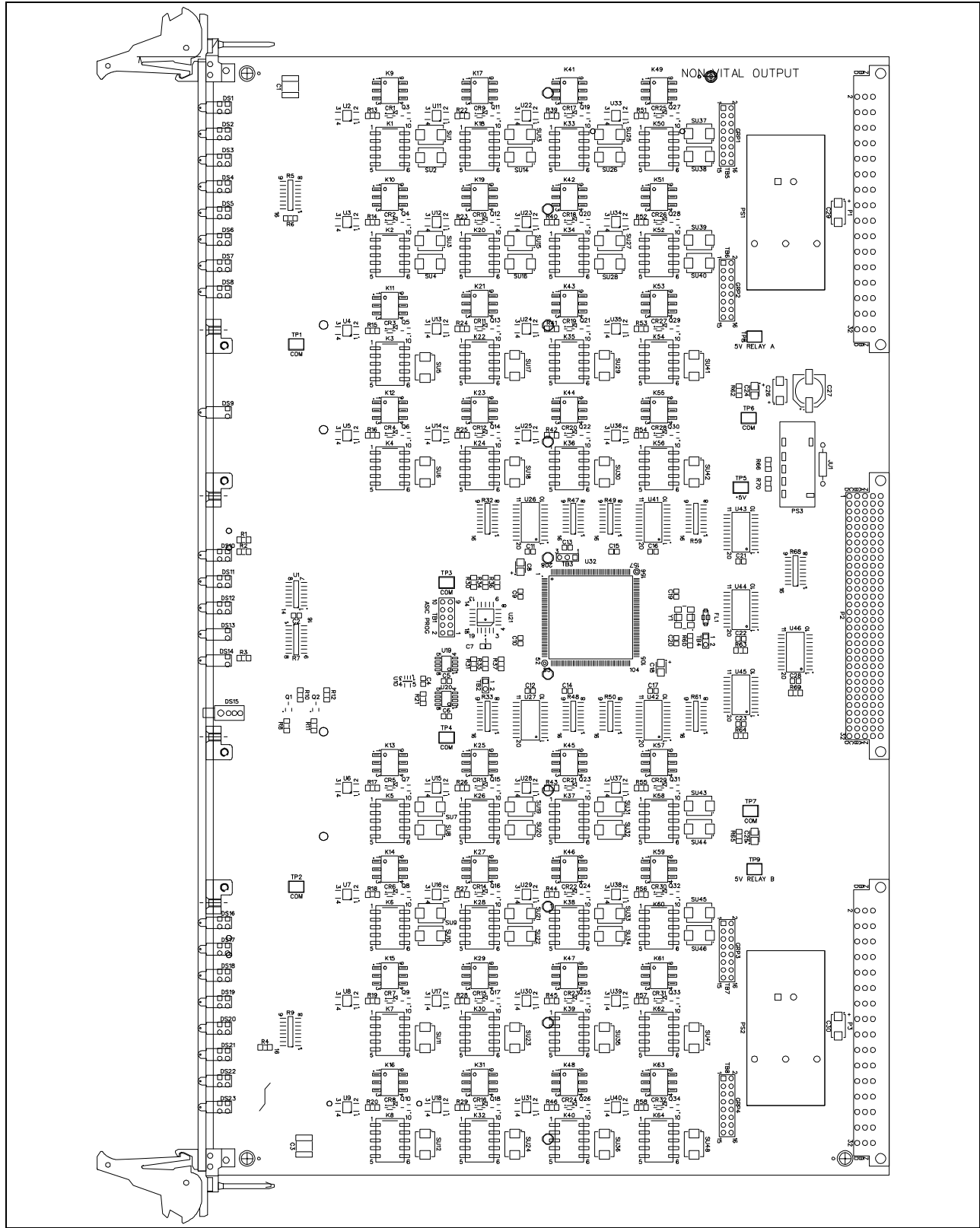


Figure A-3. NVO Board, P/N 31166-458-01 and -02

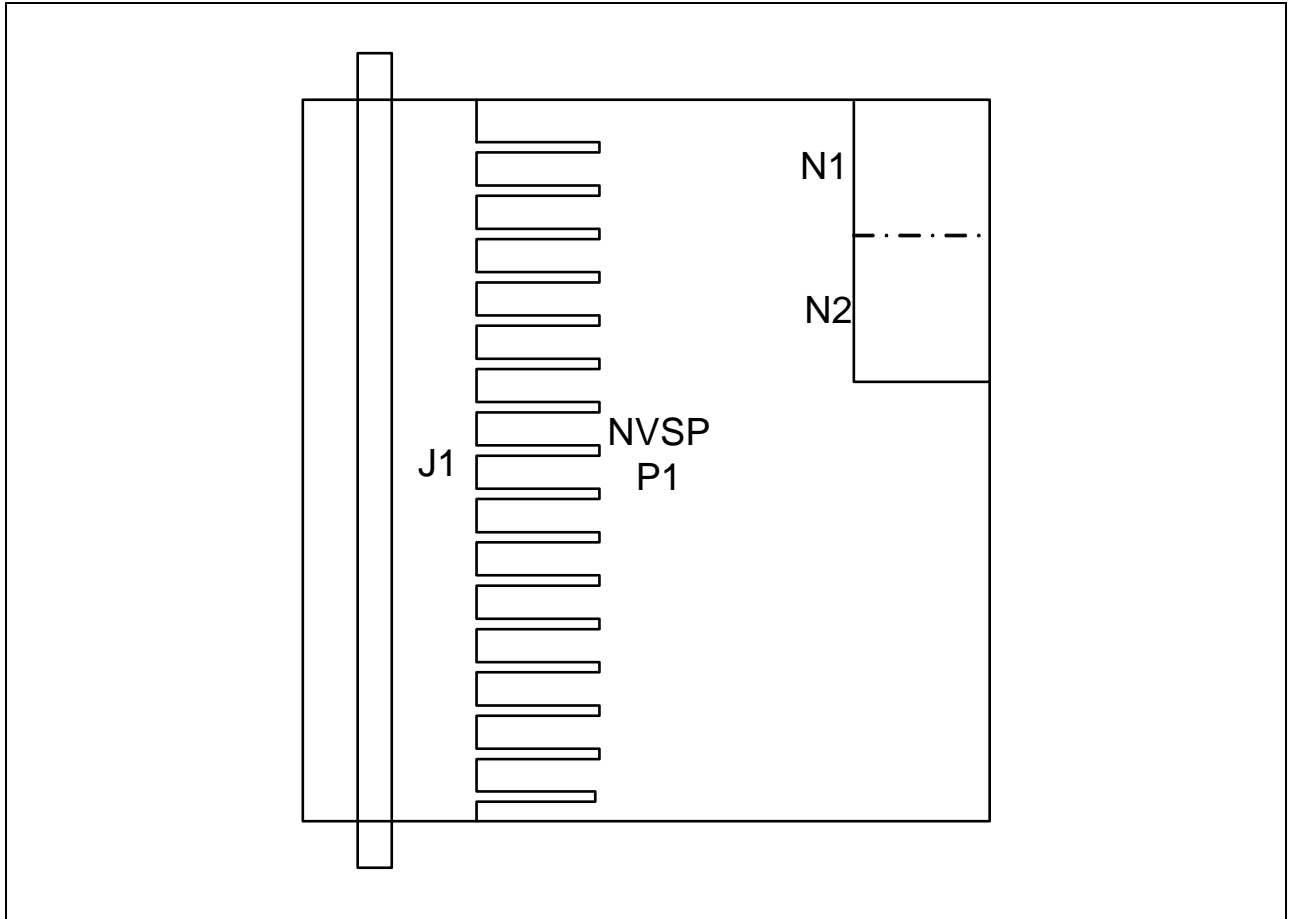


Figure A-4. NVSP P1 Interface Board, P/N 31166-474-01

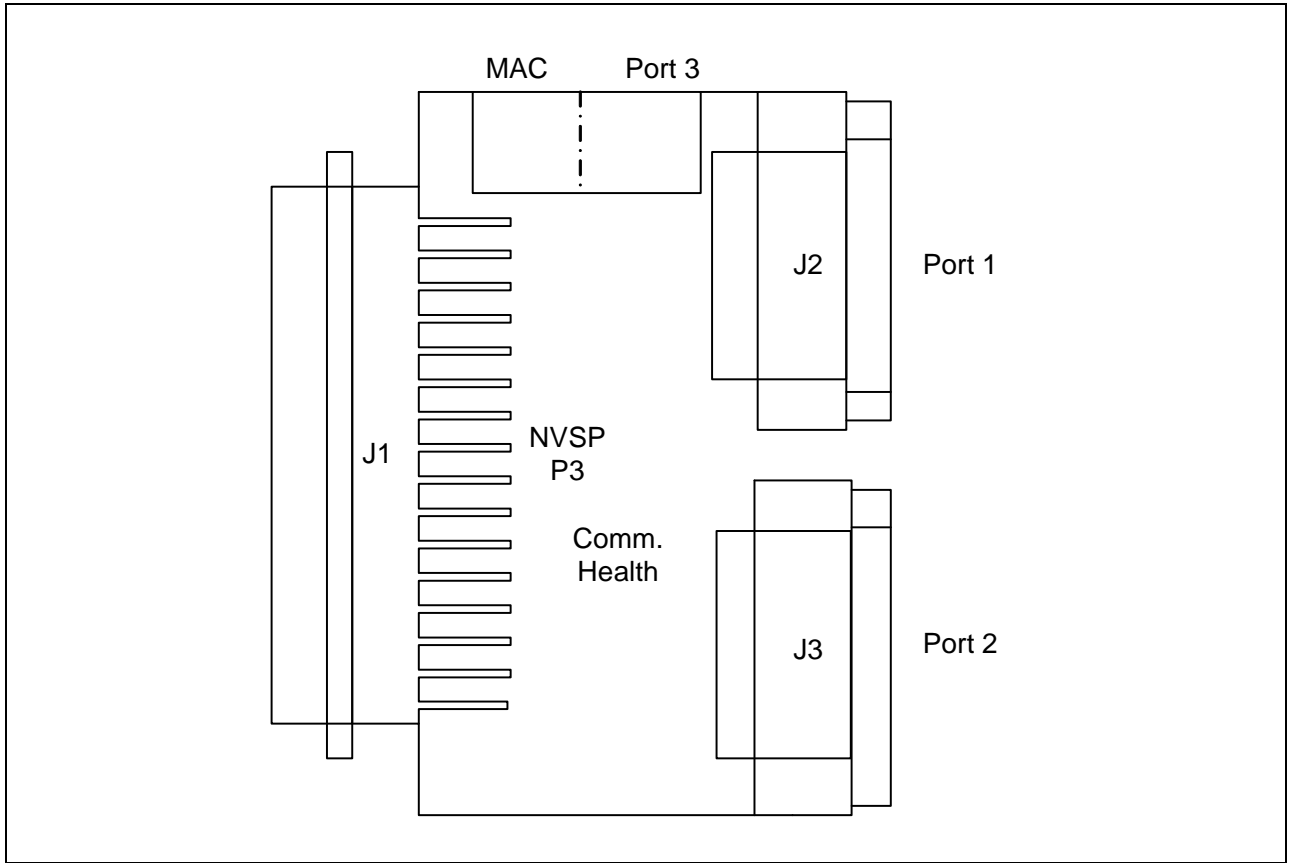


Figure A-5. NVSP P3 Interface Board, P/N 31166-475-01



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