



VPI[®] II

Vital Processor
Interlocking Control
System

Non-Vital Subsystem

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Non-Vital Subsystem Manual
P2511B, Volume 4



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PREFACE

NOTICE OF CONFIDENTIAL INFORMATION

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ABOUT THE MANUAL

This manual is intended to describe the Alstom Vital Processor Interlocking Control System, (VPI® II) non-vital subsystem (non-vital boards). This manual is part of a 5 volume set of manuals. The set is summarized in Section 1.

The information in this manual is arranged into sections. The title and a brief description of each section follow:

Section 1 – NON-VITAL PRINTED CIRCUIT BOARDS: This section summarizes the VPI® II non-vital subsystem boards.

Section 2 – CSEX3 (CODE SYSTEM EMULATOR EXTENDED 3) BOARD, P/N 31166-175-XX: This section provides CSEX3 board detail.

Section 3 – NVI (NON-VITAL INPUT) BOARD P/N 59473-757-XX: This section provides NVI board detail.

Section 4 – NVIDSW (NON-VITAL INPUT DIFFERENTIAL SWITCH) BOARD P/N 31166-276-XX: This section provides NVIDSW board detail.

Section 5 – NVO (NON-VITAL OUTPUT) BOARDS P/N 59473-785-XX and 59473-936-XX: This section provides NVO and NVOAC board detail.

Section 6 – NVO-SNK (NON-VITAL OUTPUT SINK) BOARD, P/N 31166-123-XX: This section provides NVO-SNK board detail.

Section 7 – NVR (NON-VITAL RELAY OUTPUT) BOARD P/N 31166-238-XX: This section provides NVR board detail.

Section 8 – NVTWC-FSK (NON-VITAL TWC FREQUENCY SHIFT KEYING) BOARD P/N 31166-119-XX: This section provides NVTWC-FSK output board detail.

Section 9 – NVTWC-MOD (NON-VITAL TWC MODEM) BOARD, P/N 31166-099-XX: This section provides NVTWC-MOD board detail.

Section 10 – NVTWC-MUX (NON-VITAL TWC MULTIPLEXER) BOARD, P/N 31166-100-XX: This section provides NVTWC-MUX board detail.

Appendix A – NON-VITAL BOARD LAYOUT DRAWINGS: This section provides the layout drawings for each non-vital board type.

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MANUAL SPECIAL NOTATIONS

In the Alstom manuals, there are three methods used to convey special informational notations to the reader. These notations are warnings, cautions, and notes. Both warnings and cautions are readily noticeable by boldface type two lines beneath the caption.

Warning

A warning is the most important notation to heed. A warning is used to tell the reader that special attention needs to be paid to the message because if the instructions or advice is not followed when working on the equipment then the result could be either serious harm or death. The sudden, unexpected operation of a switch machine, for example, or the technician contacting the third rail could lead to personal injury or death. An example of a typical warning notice follows:

WARNING

DISCONNECT MOTOR ENERGY WHENEVER WORKING ON SWITCH LAYOUT OR SWITCH MACHINE. UNEXPECTED OPERATION OF MACHINE COULD CAUSE INJURY FROM OPEN GEARS, ELECTRICAL SHOCK, OR MOVING SWITCH POINTS.

Caution

A caution statement is used when an operating or maintenance procedure, practice, condition, or statement, which if not strictly adhered to, could result in damage to or destruction of equipment. A typical caution found in a manual is as follows:

CAUTION

Turn power off before attempting to remove or insert circuit boards into a module. Boards can be damaged if power is not turned off.

Note

A note is normally used to provide minor additional information to the reader to explain the reason for a given step in a test procedure or to just provide a background detail. An example of the use of a note follows:

NOTE

A capacitor may be mounted on the circuit board with a RTV adhesive. Use the same color RTV.

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1. SECTION 1 – NON-VITAL PRINTED CIRCUIT BOARDS

1.1. INTRODUCTION

This manual describes the Printed Circuit Boards used to provide non-vital functionality in the VPI II System. It includes a brief description of the differences between board variations and the keying information for all variations of each board type.

1.2. MANUAL SET ORGANIZATION

This manual is part of a 5 volume set supporting the VPI II system. The set is organized as follows:

- Volume 1, Installation, Operation, and Theory Manual, includes general overview of the field installation and setup of the VPI II system; including capacity guidelines and allowable VSC/ CSEX3 Board combinations, system operation, and theory of operation.
- Volume 2, Chassis Configuration, describes the chassis configuration including cables and power supplies.
- Volume 3, Vital Subsystem, includes the Vital subsystem board drawings, signature headers and proms, and board reference data.
- Volume 4, Non-Vital Subsystem, is this document. It includes non-vital subsystem board drawings and board reference data.
- Volume 5, Maintenance and Troubleshooting, describes system maintenance and troubleshooting, including discussion of diagnostics and references for the applicable software and hardware manuals.

1.3. NON-VITAL SUBSYSTEM

Figure 1–1 is a block diagram of the boards in the non-vital subsystem.

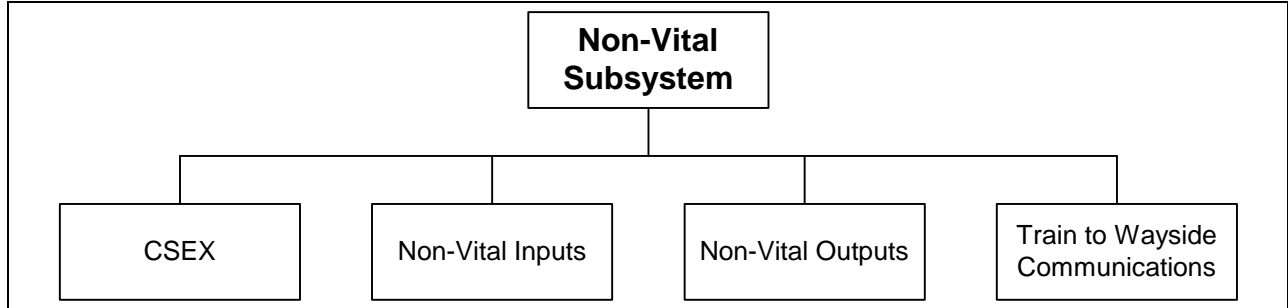


Figure 1–1. Non-Vital Subsystem

Table 1–1 lists the non-vital printed circuit boards in the order that they are discussed. A board's 10 digit drawing number is also the part number use for ordering the board.

Table 1–1. Non-Vital Printed Circuit Boards Index

Board Type	Drawing Number	Comments
CSEX3	31166-175-02	6 Serial Ports
CSEX3	31166-175-03	DC Code Line + 5 Serial Ports
NVI	59473-757-02	32 inputs, 18-33 VDC Source Inputs
NVI	59473-757-03	32 inputs, 9-18 VDC Source Inputs
NVIDSW	31166-276-01	32 inputs w/Force Input Switch, 9-18 VDC Source
NVIDSW	31166-276-02	32 inputs, 9-18 VDC Source Inputs
NVIDSW	31166-276-03	32 inputs w/Force Input Switch, 18-33 VDC Source
NVIDSW	31166-276-04	32 inputs, 18-33 VDC Source Inputs
NVO	59473-785-01	32 outputs, 18-33 VDC, 0.25 A, Source Outputs
NVO	59473-785-02	32 outputs, 9-18 VDC, 0.25 A, Source Outputs
NVO	59473-785-03	32 outputs, 18-33 VDC, 0.25 A Source Outputs, Power On Reset
NVO	59473-785-04	32 outputs, 9-18 VDC, 0.25 A, Source Outputs, Power On Reset
NVO	59473-785-05	32 outputs, 4.5 - 14.5 VDC, 0.25 A, Source, Power On Reset
NVOAC	59473-936-01	32 outputs, 5-250 VAC, 0.25 A, 47-70 HZ
NVOAC	59473-936-02	32 outputs, 5-250 VAC, 0.25 A, 47-70 HZ, Power On Reset
NVO-SNK	31166-123-01	32 outputs, 4.5 - 14.5 VDC, 0.25 A, Sink Outputs, Power On Reset
NVR	31166-238-01	32 outputs, for use with 9 - 18 VDC power supply for relays
NVR	31166-238-02	32 outputs, for use with 18 - 35 VDC power supply for relays
NVTWC-FSK	31166-119-02	4 Channel Receive Only (analog) w/40025-238-00 TWC software, processor based TWC
NVTWC-FSK	31166-119-03	4 Channel Transmit/Receive (analog) w/40025-242-00 TWC software, processor based TWC
NVTWC-FSK	31166-119-04	4 Channel Transmit/Receive (analog) w/40025-284-00 TWC software, processor based TWC
NVTWC-FSK	31166-119-05	4 Channel Transmit/Receive (analog) w/40025-289-00 TWC software, processor based TWC

Table 1–1. Non-Vital Printed Circuit Boards Index (Cont.)

Board Type	Drawing Number	Comments
NVTWC-FSK	31166-119-06	4 Channel Transmit/Receive (analog) w/40025-295-00 TWC software, processor based TWC
NVTWC-MOD	31166-099-02	2 Channel TWC Transmit/Receive (Analog) w/40026-237-00 TWC software, processor based
NVTWC-MUX	31166-100-02	4 Channel TWC Transmit/Receive (Digital) Multiplexer w/40026-236-00 TWC software, processor based TWC

Each board contains three card edge connectors, identified as P3, P2 and P1 from top to bottom. These connections are described for each system board in the sections that follow. For the user defined inputs and outputs, refer to the .lvc output file generated by the system software CAAPE program. For additional information on this program, refer to the following Alstom manuals:

- P2412A, CAAPE Users Guide
- P2412B, CAAPE AlsDload
- P2412D, VPI CAA Reference

1.4. NON-VITAL PROCESSOR FAMILY (NVP)

The non-vital processors perform important communications, data logging and non-vital logic operations within the VPI II system. There have been three generations of processor boards with generally increasing functionality. All the non-vital processors are referred to as CSEX, which stands for Code System Emulator eXtended. The VPI II system uses the CSEX3 board.

The first CSEX board family was the P/N 59473-938-XX series. This board was developed to support multiple, non-vital communications links simultaneously and to permit the separation of the non-vital application from the Vital to better support the non-vital application requirements. The CSEX2 board family, P/N 31166-049-XX series, enhanced the flexibility of configuration of the non-vital communications interfaces and the first generation of data logging. The latest family, CSEX3, P/N 31166-175-XX series, was designed to support larger, more demanding non-vital applications and provided a greater depth of memory for data logging. The CSEX3 was also designed to be a plug-in replacement for either the earlier CSEX or CSEX2 board assemblies.

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2. SECTION 2 – CSEX3 (CODE SYSTEM EMULATOR EXTENDED 3) BOARD, P/N 31166-175-XX

2.1. GENERAL

The CSEX3 (Code System Emulator eXtended) Board is designed as a system board for VPI II as well as a stand-alone non-vital logic processor. The CSEX3 board has six serial ports for communications to external devices, such as modems, other CSEX3 boards, etc. A DC code line interface is available as well as EIA232, EIA422 and EIA485 interfaces. The CSEX3 board provides an interface to non-vital inputs and outputs for local control of an interlocking. Battery-backed RAM and a Real Time Clock are included for data logging.

2.2. FEATURES

The following is a brief description of CSEX3 major features.

Serial Ports: 6 ports total. Up to a 56K baud rate is available on all serial ports. All serial ports are optically isolated from the logic power. Serial ports 1-5 also contain suppression diodes to protect the CSEX3 board from power surges on the communication lines. The P3 connector is used to access serial ports 1-5.

- Serial ports 1 and 2 support synchronous and asynchronous EIA232, EIA422 and EIA485. Serial port 2 can alternately support a DC code line.
- Serial ports 3-5 support asynchronous EIA422 and EIA485.
- Serial Port 6 supports asynchronous EIA232, available at the front DB-9 connector or from the backplane. Serial port 6 is the MAC (Maintenance ACcess) port used for connecting to a diagnostic terminal or personal computer for on-line diagnostic purposes.

Future upgrade: Different versions of the P3 Auxiliary Board may be designed for expanded communications capability. The address/data bus from the CPU is available for use on the Auxiliary Board.

Diagnostic port: Port for connection to a logic analyzer.

RAM: 2 Mbytes (1 Mbyte system RAM and 1 Mbyte BBRAM).

ROM: 1 Mbyte Flash ROM.

CPU: Intel 80C186EB running at 20 MHz.

Watchdog: resets the CPU if system power fails, if the software does not periodically address the watchdog, or if the reset button (SW8) is pressed.

Real-Time Clock (RTC): Used to keep system time. The RTC is battery-backed to keep time when power is removed. The accuracy of the RTC is dependent on the accuracy of the crystal. At 25°C, the worst-case deviation is approximately 1 minute/month.

DC-DC Converter: Provides isolated 5 volt power to operate the isolated components of the serial ports.

Dual-Ported RAM: 2 Kbytes used for a message buffer for communications with VPI II's CPU II Board.

Board-Edge Diagnostics: Status LEDs to indicate various parameters and two 7-segment displays (controlled by a three-position switch).

Non-Vital I/O: The CSEX3 board is designed to control non-vital I/O boards, including non-vital TWC (Train-to-Wayside Communications) Boards.

Battery: Easily changeable lithium button cell, with a minimum life of 48 hours for maintaining the RTC and battery-backed RAM contents when external power is removed.

2.3. OPERATION

The CSEX3 board provides the non-vital logic functions within the Alstom VPI II system chassis. This board can receive Vital indicator data from and pass control data to the VPI II Vital application logic via a dual port memory interface (DPRAM), as shown in Figure 2–1.

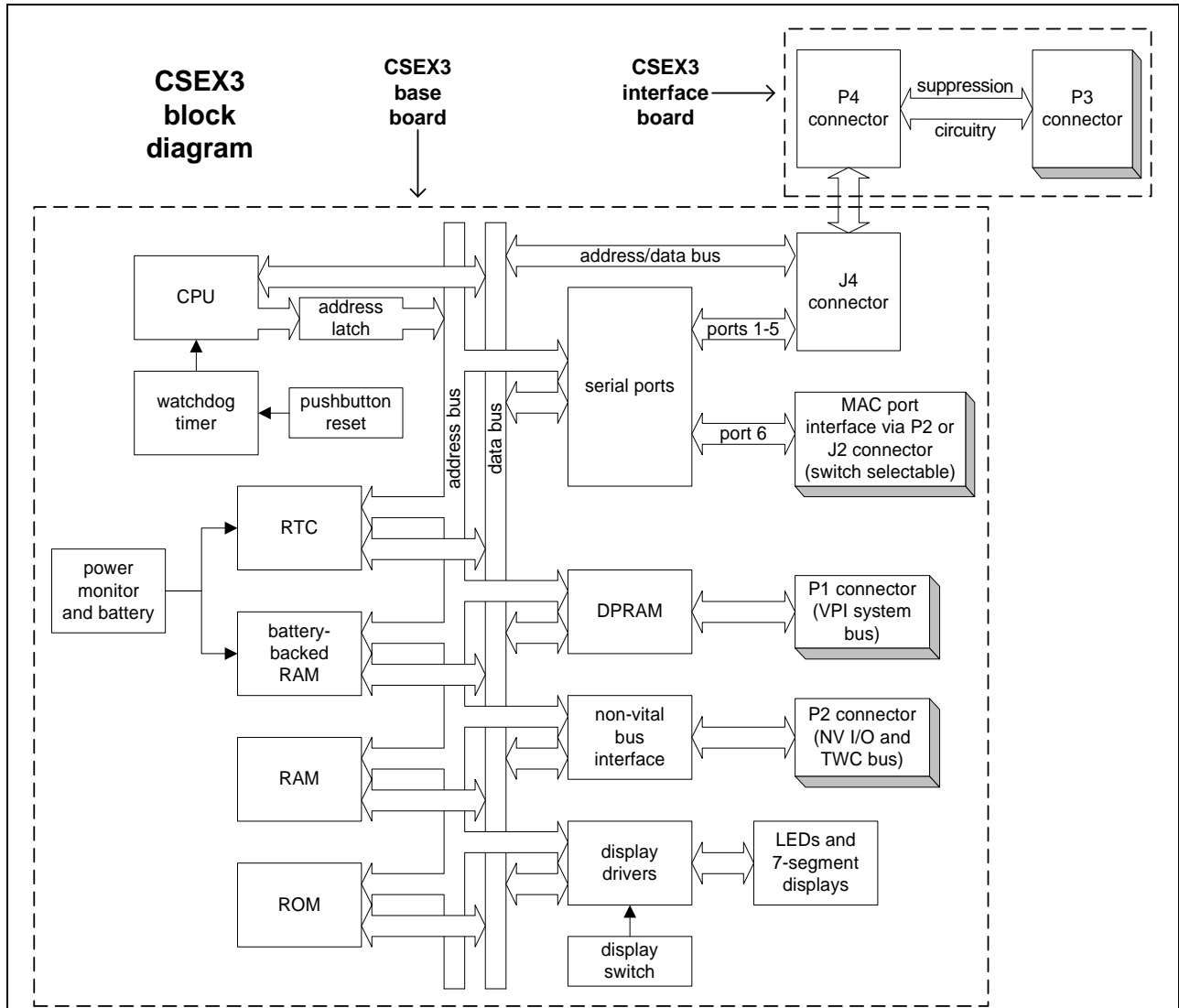


Figure 2–1. CSEX3 Board Block Diagram

2.4. STATUS AND ACTIVITY INDICATORS

The CSEX3 board has twenty LED indicators to display the status of the board, the software and the communication ports. Figure 2–2 shows the location of the LED indicators, while Table 2–1 summarizes the function of the LEDs. The information in this table assumes that the LEDs are not being used by the operator for diagnostics accessible using diagnostic switch SW11 (see “Diagnostic Display and Switch” later in this section).




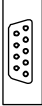

























NORMAL INDICATION	PCB NOTATION	FUNCTION
ON	DS1	 ISO5V (Isolated +5V Power)
	SW1	 F B MAC F/B (Maintenance Port Selection Front or Back of Board)
	TP3	 +5V (+5 Volts Test Point)
	J3	 (MAC Port)
	TP4	 COM (Common Test Point)
ON	DS2	 PWR (System +5V Power)
ON	DS3	 RUN (System Running)
ON	DS4	 APPL EXEC (Application Running)
	SW8	 RESET (Reset Switch)
ON, OFF	DS5	 5TX (Channel 5 Transmit)
ON, OFF	DS6	 5RX (Channel 5 Receive)
OFF	DS7	 4TX (Channel 4 Transmit)
OFF	DS8	 4RX (Channel 4 Receive)
OFF	DS9	 3TX (Channel 3 Transmit)
OFF	DS10	 3RX (Channel 3 Receive)
	TP5	 FL WR EN (Flash Write Enable Test Point)
OFF	DS11	 2NORMAL (Channel 2, Future Use)
OFF	DS12	 2RX ERROR (Channel 2 Receive Error Condition)
OFF	DS13	 2INVAL ADDR (Channel 2 Invalid Address)
OFF	DS14	 2RESPONSE (Channel 2 Is Transmitting)
OFF	DS15	 2ADDR OK (Channel 2 Valid Address Received)
OFF	DS16	 1NORMAL (Channel 1, Future Use)
OFF	DS17	 1RX ERROR (Channel 1 Receive Error Condition)
OFF	DS18	 1INVAL ADDR (Channel 1 Invalid Address)
ON, OFF	DS19	 1RESPONSE (Channel 1 Is Transmitting)
ON, OFF	DS20	 1ADDR OK (Channel 1 Valid Address Received)
	DS21	 7-Segment Diagnostic Displays
	DS22	 7-Segment Diagnostic Displays
	SW11	 ENTER / SELECT

Figure 2–2. CSEX3 Board Edge

Table 2–1. CSEX3 Board LED Descriptions

LED	Label on Board	Function
DS1	ISO5V	isolated 5V is present
DS2	PWR	board power is present
DS3	RUN	CPU is running; flashes when a CPU reset occurs
DS4	APPL EXEC	non-vital application (NVA) logic is running
DS5	5TX	serial port 5 transmitting data
DS6	5RX	serial port 5 receiving data
DS7	4TX	serial port 4 transmitting data
DS8	4RX	serial port 4 receiving data
DS9	3TX	serial port 3 transmitting data
DS10	3RX	serial port 3 receiving data
DS11	2NORMAL	not used (reserved for future use)
DS12	2RX ERROR	serial port 2 error in received message
DS13	2INVAL ADDR	serial port 2 invalid (unknown) address in received message
DS14	2RESPONSE	serial port 2 transmitting data
DS15	2ADDR OK	serial port 2 valid addressed message received
DS16	1NORMAL	not used (reserved for future use)
DS17	1RX ERROR	serial port 1 error in received message
DS18	1INVAL ADDR	serial port 1 invalid (unknown) address in received message
DS19	1RESPONSE	serial port 1 transmitting data
DS20	1ADDR OK	serial port 1 valid addressed message received

2.5. TEST POINTS

Table 2–2 describes the test points on the CSEX3 Board. Oscilloscope and clip leads may be temporarily attached to the board using the test points. TP3, TP4, and TP5 are always accessible, even when the board is in a system. See Figure 2–3 for an illustration of the CSEX3 board including test point locations.

Table 2–2. CSEX3 Board Test Points

Test Point	Label	Connection
TP1	ISO5V	isolated +5V power
TP2	ISOCOM	isolated common
TP3, TP7, TP9	+5V	+5V power
TP4, TP6, TP8	COM	common
TP5	FL WR EN/	reserved for future use

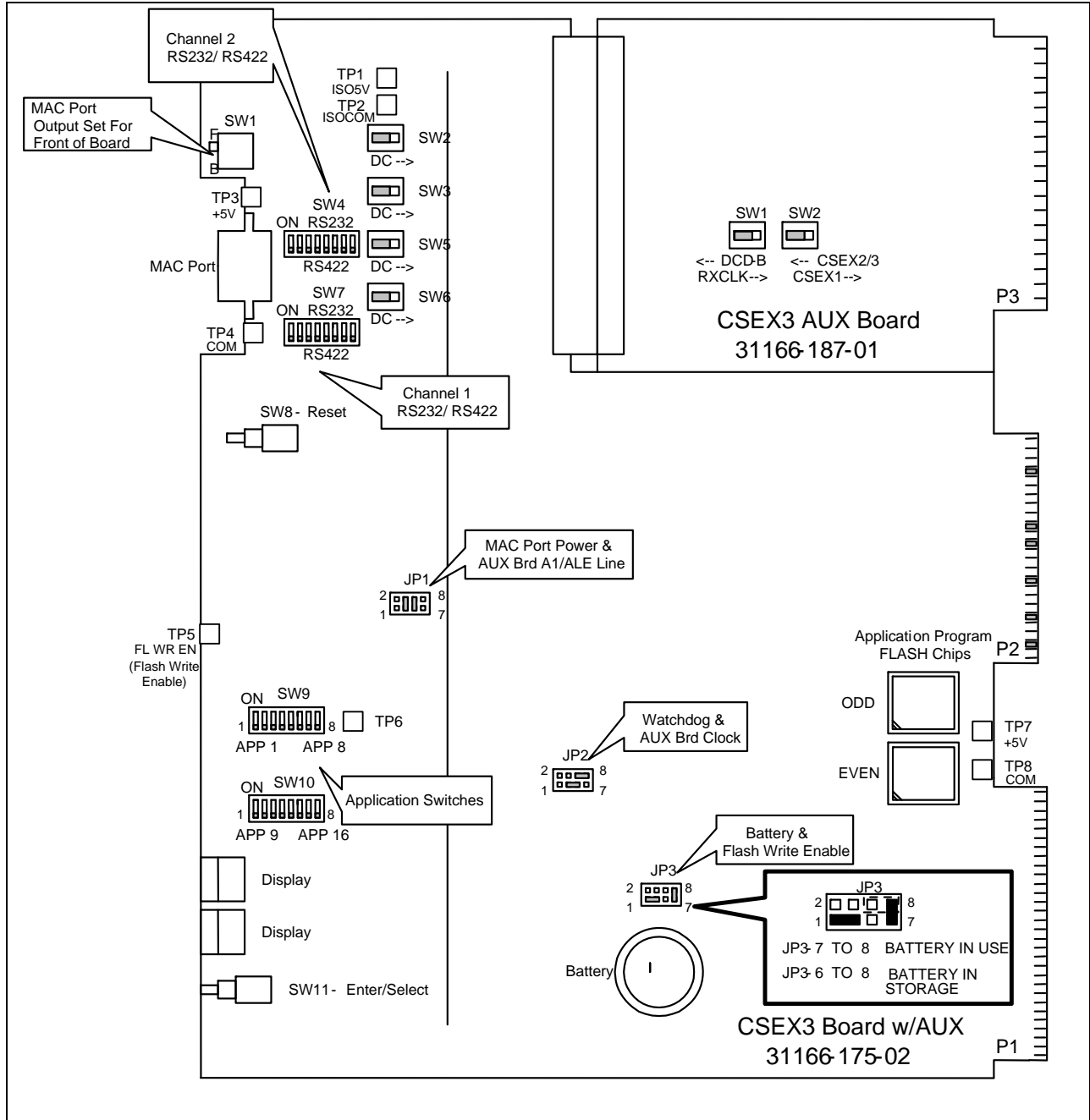


Figure 2–3. CSEX3 Board Port, Switches, Test Point Locations

2.6. JUMPERS

Tables 2–3 through 2–8 show the jumper assignments for the CSEX3 Board. All possible functions have a jumper installed even though the jumper may not make an electrical connection. This is done to ensure that there is the correct number of jumpers (six) on the board at all times. See Figure 2–3 for an illustration of the CSEX3 board including jumper locations.

Table 2–3. CSEX3 Board MAC Port Power Selection Jumper

JP1	Function
3-4	5 volt power not connected to J3, jumper installed
1-2	5 volt power connected to J3 (do not use), remove if installed, see warning on page 2–12

Table 2–4. CSEX3 Board Auxiliary Board Selection Jumper

JP1	Function
5-6	no auxiliary board A1/ALE selected (normal position), jumper installed
6-8	ALE signal line selected to AUX board
7-8	A1 signal line selected to AUX board

Table 2–5. CSEX3 Board Watchdog Selection Jumper

JP2	Function
3-5	enable watchdog reset (normal operation) , jumper installed
1-3	disable watchdog reset (for emulator use only)

Table 2–6. CSEX3 Board Auxiliary Board Clock Rate Selection Jumper

JP2	Function
2-4	auxiliary board clock rate 14.7456 MHz selected
4-6	auxiliary board clock rate 20 MHz selected
6-8	auxiliary board clock rate none selected, jumper installed

Table 2–7. CSEX3 Board Battery Selection Jumper

JP3	Function
6-8	battery disconnected (use this position for shipping and storage, or if no battery is installed during operation)
7-8	battery connected (do not use this position if no battery is installed)

Table 2–8. CSEX3 Board Flash Enable Jumper

JP3	Function
1-3	Flash Write always disabled
3-4	Flash Write always enabled
2-4	Flash Write enabled by TP5 only

2.7. SERIAL PORTS

All serial ports are powered by an on-board isolated 5V-5V DC-DC converter. Both the 5V and common outputs of the DC-DC converter are completely isolated from the rest of the circuit. When replacing a CSEX1 or CSEX2 Board, the off-board power supply used to power CSEX1 or CSEX2 communications may either be left connected (the incoming power pin is not connected on CSEX3), or it may be removed (if no other boards are relying on the power supply).

Serial ports 1 and 2 can receive and transmit the EIA232, EIA422 and EIA485 standards. Serial port 2 can also be alternately configured as a DC code line interface. Both ports can be configured independently, as shown in Table 2–9 through 2–11. Serial ports 3 through 5 can receive and transmit the EIA422 and EIA485 standards. See Figure 2–3 for an illustration of the CSEX3 board including switch locations.

Table 2–9. CSEX3 Board Channel 1 Communication Standard Selection Switch Setting

Standard	SW7 Position
EIA422/485	all off
EIA232	all on

Table 2–10. CSEX3 Board Channel 2 Communication Standard Selection Switch Setting

Standard	SW4 Position
EIA422/485	all off
EIA232	all on

Table 2–11. CSEX3 Board Port 2 DC Code Line Communication Selection Switch Setting

Communication Mode	SW2, SW3, SW5 and SW6 Position
EIA232/422/485	all switch actuators towards front of board
DC code line	all switch actuators towards back of board, displayed on board by DC→

Serial port 6 (the MAC port) receives and transmits the EIA232 standard, and is used to connect diagnostic equipment, such as a laptop computer, to the CSEX3 Board. Switch SW1 determines whether the MAC ports RXD signal (an input to the CSEX3 Board) is accessible through the DB-9 connector at the front of the board, or through the backplane (for a permanent diagnostic connection). The MAC port's TXD signal always transmits data to both the front and the back of the board. Table 2–12 describes the MAC port connections through the DB-9 connector, and Table 2–13 describes the switch settings to select between front and back MAC port access.

Table 2–12. CSEX3 Board MAC Port Connector Pin Assignments

Pin	Function
J3-1	-
J3-2	RXD: receive data
J3-3	TXD: transmit data
J3-4	-
J3-5	ISOCOM: isolated common
J3-6	-
J3-7	-
J3-8	-
J3-9	ISO5V: isolated +5V (only when the proper jumper is installed) see warning below

WARNING

CONNECTION TO PIN J3-9 IS NOT RECOMMENDED UNLESS THE DEVICE USING THIS POWER IS APPROVED FOR USE. EXCESSIVE CURRENT DRAWN FROM THIS PIN CAN AFFECT THE OPERATION OF THE CSEX3 BOARD.

Table 2–13. CSEX3 Board MAC Port RXD Source Selection Switch Setting

SW1 Setting	Source
"F"	front of board (DB-9 connector)
"B"	backplane connection

2.8. DIAGNOSTIC DISPLAY AND SWITCH

The CSEX3 board offers a 2-digit diagnostic display used in conjunction with a 3-position diagnostic input switch through which various diagnostic functions may be accessed.

When the CSEX3 board is turned on, the diagnostic display (labeled DS21 and DS22) normally displays "8.8." for a moment followed by "0 0". Other displayed codes indicate an operational problem that resulted in a system reset.

To operate the display, use switch SW11, shown in Figure 2–2. The ENTER (up) position is used to enter or exit a diagnostic function. The SELECT (down) position is used to advance to the next diagnostic function and to make selections.

The diagnostic display can be used in conjunction with two sets of CSEX3 board edge LEDs, labeled DS12 through DS15 and DS17 through DS20, to view the status of non-vital I/O ports and represent an I/O group of 8 ports. When not being used for diagnostic purposes, these LEDs are used to show communication activity on ports 1 and 2 (see Table 2–14).

Each non-vital I/O board is comprised of 32 ports consisting of four groups of 8 ports per board. To access an output, use the SELECT function to advance to the appropriate I/O board and group. The output board and group numbers start with 0.0 (as shown on the diagnostic display), whereas the input board and group numbers are offset by one and therefore start at 1.0 (input board #1, group 0). Depress SELECT repeatedly to advancing through output groups: 0.0 through 0.3 for the first board, 0.4 through 0.7 for second board, 0.8 through 1.1 for third and so on. When each I/O board and group is selected, the 8 LEDs display the status of that group's I/O ports in real time. The LEDs are read from bottom to top, which is the reverse order with respect to the layout of ports on the I/O boards themselves.

Table 2–14. CSEX3 Board Diagnostic Display and Switch

Diagnostic Function	Description
00	No diagnostic function is currently selected. LEDs DS12-DS15 and DS17-DS20 shows communication port activity, as is the normal operational use of these LEDs.
01	Show the total number of system resets since power-up, displayed in the form “02.” for example.
02	Test LEDs DS12-DS15 and DS17-DS20 by incrementally lighting each in a binary pattern upon each press of SELECT.
03	Display the current state of the DC codeline relay, and test LEDs as in diagnostic function 02.
04	Use LEDs DS12-DS15 and DS17-DS20 to show the current state of a group of 8 non-vital inputs; advance to the next input group or board by pressing SELECT.
05	Use LEDs DS12-DS15 and DS17-DS20 to show the current state of a group of 8 non-vital outputs; advance to the next output group or board by pressing SELECT.
06	Perform a system reset; displays “RE” (reset) when this function is entered. To reset the CSEX3 board press SELECT, else press ENTER to abort. After a reset thus induced, the diagnostic display shows “1d”.

2.9. TROUBLESHOOTING GUIDE

Table 2–15. CSEX3 Board Troubleshooting Guide

Observation	Possible Cause
All LEDs are off	No +5V ($\pm 0.25V$) system power.
Status of LEDs does not change	Communication port interface problem.
The “Application Is Running” LED does not light	The non-vital application code is not operational.
The “CPU Is Running” LED flashes on and off	The operating software is not running correctly - verify proper programming of EPROMs.
Controls or displays do not function as expected	CAA application logic programming or wiring error.
Maintenance (MAC) port does not operate properly	Check the error code shown on the 2-digit diagnostic display. Check the MAC port for communication activity. Verify wiring of the MAC port cable.

2.10. CARD EDGE CONNECTORS

The CSEX3 Board has three card edge connectors:

- P3, the top connector, is actually located on the interchangeable auxiliary board and available in 36-pin and 60-pin configurations (determined by auxiliary board); it is used to access serial ports 1 through 5
 - See Tables 2–16 through 2–18 for 36-pin configuration details
 - See Tables 2–19 and 2–20 for 60-pin configuration details
- P2, the middle connector, is a 50-pin connector used to interface with NV I/O and TWC boards, and the +5V power is supplied on the P2
 - P2-42 through P2-47 are wired in a specific pattern to common P2-48 per the application .lvc CAAPE report for board addressing; the remaining P2 pins are not user configurable
- P1, the lower connector, is a 36-pin connector which interfaces with the VPI II system bus
 - See Table 2–21 for 36-pin configuration details

NOTE

For the user defined inputs and outputs, refer to the .lvc output file generated by the system software CAAPE program.

Table 2–16. CSEX3 Board 36-pin P3 Connections

P3-	Name	Dir.	EIA232	EIA422 / EIA485	DC code line	ARES (EIA232)	ATCS (EIA422)
1	NC						
2	ISOCOM						
3	NC/ISOCOM						
4	1TXD-A	O	✓	✓		✓	✓
5	1TXD-B	O		✓			✓
6	1RTS-A	O	✓	✓		✓	1TXCLK-A
7	1RTS-B	O		✓			1TXCLK-B
8	1RXD-A	I	✓	✓		✓	✓
9	1RXD-B	I		✓			✓
10	1CTS-A	I	✓	✓		✓	
11	1CTS-B	I		✓			
12	1DCD-A	I	✓	✓		1TXCLK	1RXCLK-A
13	1DCD-B	I		✓		1RXCLK	1RXCLK-B
14	2TXD-A	O	✓	✓	TX_V+	✓	✓
15	2TXD-B	O		✓	TX_V-		✓
16	2RTS-A	O	✓	✓	TX1	✓	2TXCLK-A
17	2RTS-B	O		✓	TX2		2TXCLK-B
18	2RXD-A	I	✓	✓	RX1+	✓	✓
19	2RXD-B	I		✓	RX1-		✓
20	2CTS-A	I	✓	✓	RX2+	✓	
21	2CTS-B	I		✓	(RX2-)		
22	2DCD-A	I	✓	✓		2TXCLK	2RXCLK-A
23	2DCD-B	I		✓	(RX2-)	2RXCLK	2RXCLK-B
24	NC/ISOCOM						
25	3RXD-A	I		✓			
26	3RXD-B	I		✓			
27	3TXD-A	O		✓			
28	3TXD-B	O		✓			
29	4RXD-A	I		✓			

✓ Indicates that the "Name" column identifies the signal for this protocol.

Table 2–16. CSEX3 Board 36-pin P3 Connections (Cont.)

P3-	Name	Dir.	EIA232	EIA422 / EIA485	DC code line	ARES (EIA232)	ATCS (EIA422)
30	4RXD-B	I		✓			
31	4TXD-A	O		✓			
32	4TXD-B	O		✓			
33	5RXD-A	I		✓			
34	5XRD-B	I		✓			
35	5TXD-A	O		✓			
36	5TXD-B	O		✓			

✓ Indicates that the “Name” column identifies the signal for this protocol.

NOTE

For DC code line operation on the 36-pin P3 connector, the RX2- input may come from either of two pins (P3-21 or P3-23).

Switch SW1 on the 36-pin Auxiliary Board routes the incoming receive clock signal needed for some synchronous communication protocols, such as ARES.

See Table 2–17 for a description of the switch usage.

Table 2–17. CSEX3 Board 36-pin P3 Auxiliary Board Communication Selection Switch (SW1)

Switch Position	Function
Actuator towards P4 connector (indicated by DCD-B on silkscreen)	Normal operation mode (maps the P3-13 input to the DCD-B signal)
Actuator towards P3 connector (indicated by RXCLK on silkscreen)	Provides external receive synchronous clock signal (maps the P3-13 input to the RXCLK signal)

Pins P3-3 and P3-24 use switch SW2 on the 36-pin Auxiliary Board to select between NC (no connect) and ISOCOM, used for CSEX1 vs. CSEX2/3 compatibility.

See Table 2–18 for a description of the switch usage.

Table 2–18. CSEX3 Board 36-pin P3 Auxiliary Board
CSEX1 vs. CSEX2/3 Switch (SW2)

Switch Position	Function
Actuator towards P4 connector (indicated by CSEX2/3 on silkscreen)	CSEX2 and CSEX3 compatibility mode (connects P3-3 and P3-24 to ISOCOM)
Actuator towards P3 connector (indicated by CSEX1 on silkscreen)	CSEX1 compatibility mode (disconnects P3-3 and P3-24 from ISOCOM)

Table 2–19. CSEX3 Board 60-pin P3 Connections, Pins 1 - 48

P3-	Name	Dir.	EIA232	EIA422 /EIA485	DC code line	ARES (RS-232)	ATCS (RS-232)	ATCS (RS-422)
1	ISOCOM							
2	ISOCOM							
3	ISOCOM							
4	1TXD-A	O	✓	✓		✓	✓	✓
5	1TXD-B	O		✓				✓
6	1RTS-A	O	✓	✓		✓	1TXSPARE	1TXSPARE-A
7	1RTS-B	O		✓				1TXSPARE-B
8	1RXD-A	I	✓	✓		✓	✓	✓
9	1RXD-B	I		✓				✓
10	1CTS-A	I	✓	✓		✓	1RXSPARE1	1RXSPARE1-A
11	1CTS-B	I		✓				1RXSPARE1-B
12	1DCD-A	I	✓	✓		1TXCLK	1RXSPARE2	1RXSPARE2-A
13	1DCD-B	I		✓				1RXSPARE2-B
14	1TXCLK-A	O	✓	✓			✓	✓
15	1TXCLK-B	O		✓				✓
16	1RXCLK-A	I	✓	✓		✓	✓	✓
17	1RXCLK-B	I		✓				✓
18	ISOCOM							
19	2TXD-A	O	✓	✓	TX_V+	✓	✓	✓
20	2TXD-B	O		✓	TX_V-			✓
21	2RTS-A	O	✓	✓	TX1	✓	2TXSPARE	2TXSPARE-A
22	2RTS-B	O		✓	TX2			2TXSPARE-B

✓ Indicates that the “Name” column identifies the signal for this protocol.

Table 2–19. CSEX3 Board 60-pin P3 Connections, Pins 1 - 48 (Cont.)

P3-	Name	Dir.	EIA232	EIA422 /EIA485	DC code line	ARES (RS-232)	ATCS (RS-232)	ATCS (RS-422)
23	2RXD-A	I	✓	✓	RX1+	✓	✓	✓
24	2RXD-B	I		✓	RX1-			✓
25	2CTS-A	I	✓	✓	RX2+	✓	2RXSPARE1	2RXSPARE1-A
26	2CTS-B	I		✓	RX2-			2RXSPARE1-B
27	2DCD -A	I	✓	✓		2TXCLK	2RXSPARE2	2RXSPARE2-A
28	2DCD -B	I		✓				2RXSPARE2-B
29	2TXCLK-A	O	✓	✓			✓	✓
30	2TXCLK-B	O		✓				✓
31	2RXCLK-A	I	✓	✓		✓	✓	✓
32	2RXCLK-B	I		✓				✓
33	ISOCOM							
34	3RXD-A	I		✓				
35	3RXD-B	I		✓				
36	3TXD-A	O		✓				
37	3TXD-B	O		✓				
38	ISOCOM							
39	4RXD-A	I		✓				
40	4RXD-B	I		✓				
41	4TXD-A	O		✓				
42	4TXD-B	O		✓				
43	ISOCOM							
44	5RXD-A	I		✓				
45	5RXD-B	I		✓				
46	5TXD-A	O		✓				
47	5TXD-B	O		✓				
48	ISOCOM							

✓ Indicates that the “Name” column identifies the signal for this protocol.

Table 2–20. CSEX3 Board 60-pin P3 Connections, Pins 49 - 60

P3-	Name	Dir.	Echelon	Ethernet	Token Ring
49	DTRBD1	I/O	TWPR-A	ETH1	TR1
50	DTRBD2	I/O	TWPR-B	ETH2	TR2
51	DTRBD3	I/O		ETH3	TR3
52	DTRBD4	I/O		ETH4	TR4
53	DTRBD5	I/O		ETH5	TR5
54	DTRBD6	I/O		ETH6	TR6
55	DTRBD7	I/O		ETH7	TR7
56	DTRBD8	I/O		ETH8	TR8
57	DTRBD9	I/O		SPARE1	TR9
58	DTRBD10	I/O		SPARE2	SPARE
59	ISOCOM				
60	ISOCOM				

Table 2–21. CSEX3 Board 60-pin P1 Connections

P1-	Name	Function
1	VPI_D0	VPI II data bus
2	COM	ground
3	VPI_D1	VPI II data bus
4	VPI_D2	VPI II data bus
5	COM	ground
6	VPI_D3	VPI II data bus
7	VPI_D4	VPI II data bus
8	COM	ground
9	VPI_D5	VPI II data bus
10	VPI_D6	VPI II data bus
11	COM	ground
12	VPI_D7	VPI II data bus
13	VPI_D8	VPI II data bus
14	COM	ground
15	VPI_D9	VPI II data bus
16	VPI_D10	VPI II data bus
17	COM	ground
18	VPI_D11	VPI II data bus
19	VPI_D12	VPI II data bus
20	COM	ground
21	VPI_D13	VPI II data bus
22	VPI_D14	VPI II data bus
23	VPI_D15	VPI II data bus
24	COM	ground
25	VPI_RD/	VPI II read
26	COM	ground
27	VPI_WR/	VPI II write
28	COM	ground
29	VPI_DEN/	VPI II data enable
30	COM	ground

Table 2–21. CSEX3 Board 60-pin P1 Connections (Cont.)

P1-	Name	Function
31	VPI_T-R/	VPI II transmit/receive
32	COM	ground
33	VPI_MRD/	VPI II memory read
34	COM	ground
35	(none)	
36	COM	ground
37	VPI_A18	VPI II address bus
38	VPI_A17	VPI II address bus
39	VPI_A16	VPI II address bus
40	COM	ground
41	VPI_A15	VPI II address bus
42	VPI_A14	VPI II address bus
43	VPI_A13	VPI II address bus
44	COM	ground
45	VPI_A12	VPI II address bus
46	VPI_A11	VPI II address bus
47	VPI_A10	VPI II address bus
48	COM	ground
49	VPI_A9	VPI II address bus
50	VPI_A8	VPI II address bus
51	VPI_A7	VPI II address bus
52	COM	ground
53	VPI_A6	VPI II address bus
54	VPI_A5	VPI II address bus
55	VPI_A4	VPI II address bus
56	COM	ground
57	VPI_A3	VPI II address bus
58	VPI_A2	VPI II address bus
59	COM	ground
60	VPI_A1	VPI II address bus

2.11. SPECIFICATIONS

Operating temperature range: -40°C to +70°C

Storage temperature range: -55°C to +85°C

Humidity: 0% to 95% non-condensing

Table 2-22. CSEX3 Board Specifications

Specification	31166-175	
	-02	-03
Maximum Number of Boards Per VPI II System	4	
Board Slots Required	1	
Maximum Board Logic Current Supply Draw	750 mA	
Power Supply	+5V	
Voltage Range	4.75V to 5.25V	
Typical Operating Current	0.75A	
Supports 29040 Flash PROM	Yes	
No. of Sync./Async. Ports	2	1
No. of Async. Only Ports	3	3
MAC Interface	EIA232	EIA232
Network Port/Type	No	No
Daughterboard Used	31166-187-01	31166-187-02
Additional Assembly Information		DC Code Line

2.12. ASSEMBLY DIFFERENCES

Table 2–23. CSEX3 Board Assembly Differences

Complete Board Assembly	Function	Sub-Assemblies	
		Base Board	Auxiliary Board
31166-175-02	6 Serial Ports	31166-175-01	31166-187-01
31166-175-03	DC Code Line + 5 Serial Ports	31166-175-01	31166-187-02

3. SECTION 3 – NVI (NON-VITAL INPUT) BOARD, P/N 59473-757-XX

3.1. GENERAL

The Non-Vital Input (NVI) Board provides 32 isolated, Non-Vital inputs that interface through the Motherboard to the VPI II module. A CSEX3 Board, employing Non-Vital I/O control software, communicates over the Motherboard bus to the NVI Board. Input states are latched and read every 25 ms.

3.2. OPERATION

Five of the available address bus lines can access one of 20 Non-Vital I/O Boards in a VPI II module. A logic comparator compares the address on the bus with the slot-programmed address, which, if they agree, results in a BOARD SELECT signal. Another address line latches the state of all system Non-Vital inputs.

Figure 3–1 shows a block diagram of this board. Inputs are arranged into four groups of 8. Two additional address lines select each of the groups. These inputs as well as BOARD SELECT go to a control PROM.

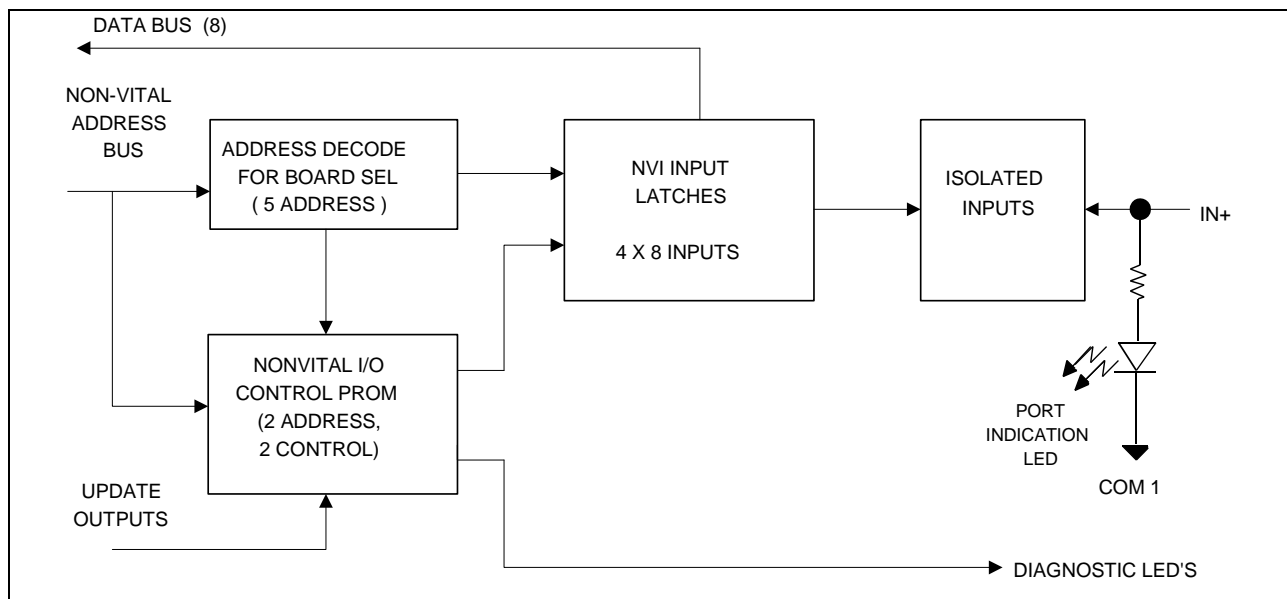


Figure 3–1. NVI Board Block Diagram

A 32 × 8 bit PROM decodes address and control line information for the execution of the latching and subsequent input read operations. Besides the above signals, memory read and Non-Vital address signals provide individual READ INPUT GROUP signals at the PROM output.

As stated, inputs are latched and read on an 8-bit basis. A LATCH address signal goes to the clock input of each of four octal latches. The READ INPUT GROUP signals enable the latch output, allowing the status of the inputs to be presented to the Non-Vital data bus.

See Figure A-2 for a board layout drawing.

3.3. ISOLATED INPUTS

Optical isolators separate the power supplies of the 5V logic system and field circuitry. Each of the four groups of 8 inputs has a separate signal return, allowing inputs derived from four isolated supplies to share one input board.

Inputs typically draw 10 mA. Secondary transient protection is provided by a resistor/metal oxide varistor pair in series with each input, thus giving protection against a transient having 3.5 joules of energy or less. In locations where inputs are subject to frequent lightning, some form of primary protection should also be used.

3.4. INDICATIONS

An indication for each input, representing the input state from the field side is found at the board's front edge, see Figure 3-2. In addition, outputs of the control PROM feed indications so that failures within address or control logic can be readily observed. Test points are also included at critical points within the circuit to assist in troubleshooting.

NORMAL INDICATION	PCB NOTATION	FUNCTION
OFF, ON	IN1	● Input #1
OFF, ON	IN2	● Input #2
OFF, ON	IN3	● Input #3
OFF, ON	IN4	● Input #4
OFF, ON	IN5	● Input #5
OFF, ON	IN6	● Input #6
OFF, ON	IN7	● Input #7
OFF, ON	IN8	● Input #8
OFF, ON	I9	● Input #9
OFF, ON	I10	● Input #10
OFF, ON	I11	● Input #11
OFF, ON	I12	● Input #12
OFF, ON	I13	● Input #13
OFF, ON	I14	● Input #14
OFF, ON	I15	● Input #15
OFF, ON	I16	● Input #16
OFF, ON	ESL	● ESL (Another Non-Vital I/O Board Is Being Accessed)
OFF, ON	ISL	● ISL (Address On I/O BUS Is Acceptable)
OFF, ON	LOH	● LCH (Input Data Is Latched)
OFF, ON	GSL	● BSL (Board Is Being Addressed By CSEX)
OFF, ON	GR4	● GR4 (Inputs 25-32 Are Being Read)
OFF, ON	GR3	● GR3 (Inputs17-24 Are Being Read)
OFF, ON	GR2	● GR2 (Inputs 9-16 Are being Read)
OFF, ON	GR1	● GR1 (Inputs1-8 Are Being Read)
OFF, ON	I17	● Input #17
OFF, ON	I18	● Input #18
OFF, ON	I19	● Input #19
OFF, ON	I20	● Input #20
OFF, ON	I21	● Input #21
OFF, ON	I22	● Input #22
OFF, ON	I23	● Input #23
OFF, ON	I24	● Input #24
OFF, ON	I25	● Input #25
OFF, ON	I26	● Input #26
OFF, ON	I27	● Input #27
OFF, ON	I28	● Input #28
OFF, ON	I29	● Input #29
OFF, ON	I30	● Input #30
OFF, ON	I31	● Input #31
OFF, ON	I32	● Input #32

IN1 - IN8 and I9 - I32: Light when energy is applied to external input.

Figure 3–2. NVI Board Edge

3.5. CARD EDGE CONNECTORS

NVI Boards have three card edge connectors:

- P3, the top connector, is a 36-pin connector which contains wiring for inputs 1 – 16 and input common connections
 - See Table 3–1 for pin configuration details
- P2, the middle connector, is a 50-pin connector used for connections to the motherboard which supplies 5 Volt power, control, data and slot addressing signals
 - P2-42 through P2-47 are wired in a specific pattern to common P2-48 per the application .lvc CAAPE report for board addressing; the remaining P2 pins are not user configurable
- P1, the lower connector, is a 36-pin connector which contains wiring for inputs 17 – 32 and input common connections
 - See Table 3–2 for pin configuration details

NOTE

For the user defined inputs and outputs, refer to the .lvc output file generated by the CAAPE program.

Table 3–1. NVI Board 36-pin P3 Connections

Input Number	P3-
1	34
2	32
3	30
4	29
5	26
6	25
7	22
8	21
COM (1-8)	36
9	18
10	17
11	14
12	13
13	10
14	9
15	6
16	5
COM (9-16)	20

Table 3–2. NVI Board 36-pin P1 Connections

Input Number	P1-
17	34
18	32
19	30
20	29
21	26
22	25
23	22
24	21
COM (17-24)	36
25	18
26	17
27	14
28	13
29	10
30	9
31	6
32	5
COM (25-32)	20

3.6. SPECIFICATIONS

Table 3–3. NVI Board Specifications

Specification	59473-757	
	-02	-03
Maximum Number of Boards Per CSEX Subsystem	20	
Board Slots Required	1	
Number of Ports Per Board	32	
Maximum Board Logic Current Supply Draw	200 mA	
Minimum Input Voltage Per Port	18.0 VDC	9.0 VDC
Maximum Input Voltage Per Port	33.0 VDC	18.0 VDC
Minimum Activation Current Per Port	10 mA (Source)	7 mA (Source)

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4. SECTION 4 – NVIDSW (NON-VITAL INPUT DIFFERENTIAL SWITCH) BOARD, P/N 31166-276-XX

4.1. GENERAL

The Non-Vital Input Differential Switch (NVIDSW) Board provides 32 isolated Non-Vital inputs to a VPI II system. Interface to the system is accomplished through the system motherboard. Input states are latched and then accessed every 25 ms. A CSEX3 board equipped with the appropriate application logic can communicate with the NVIDSW Board through the Non-Vital Data Bus. On certain NVIDSW Boards the user can mechanically set the state of the inputs through 32 switches located on the front of the board. The inputs can be forced ON, OFF or to the state of the physical input.

The state of the inputs through 32 switches located on the front of the board can be mechanically set by the user on assemblies one and three of the NVIDSW Board (P/N 31166-276-01 and 03). Assemblies two and four (P/N 31166-276-02 and 04) have no switches. Assemblies one and two are rated for a 9 to 18 input voltage range. Assemblies three and four are rated for an 18 to 33 input voltage range.

See Figure A–3 for a board layout drawing.

4.2. OPERATION

Five of the available address bus lines access one of 20 Non-Vital I/O Boards. The inputs on the NVIDSW Board are arranged in four groups of 8. Two additional address lines select each of the groups. The slot address, along with these seven address lines and two control signals are routed to an FPGA (Field Programmable Gate Array) on the board. The FPGA processes these signals to determine if the address on the bus matches the slot address of the board. If the two match, the appropriate 8 bits from one of the groups is loaded to the Non-Vital Data Bus. The FPGA also outputs signals to onboard diagnostic indications so that failures within the address and control logic can be readily observed.

In the case of the NVIDSW Boards (P/N 31166-276-01/03), the actual value of the switch overrides the value that is normally read by the FPGA on the board edge. The switches are three-position toggles, with a position assigned to allow the actual value to go through, to pull the value low, or to pull the value high. The -02 assembly and -04 assembly versions of the board do not contain these switches, and the normal value passes through unchanged in all cases.

4.3. INDICATIONS

Figure 4–1 shows the NVIDSW board LED indications.

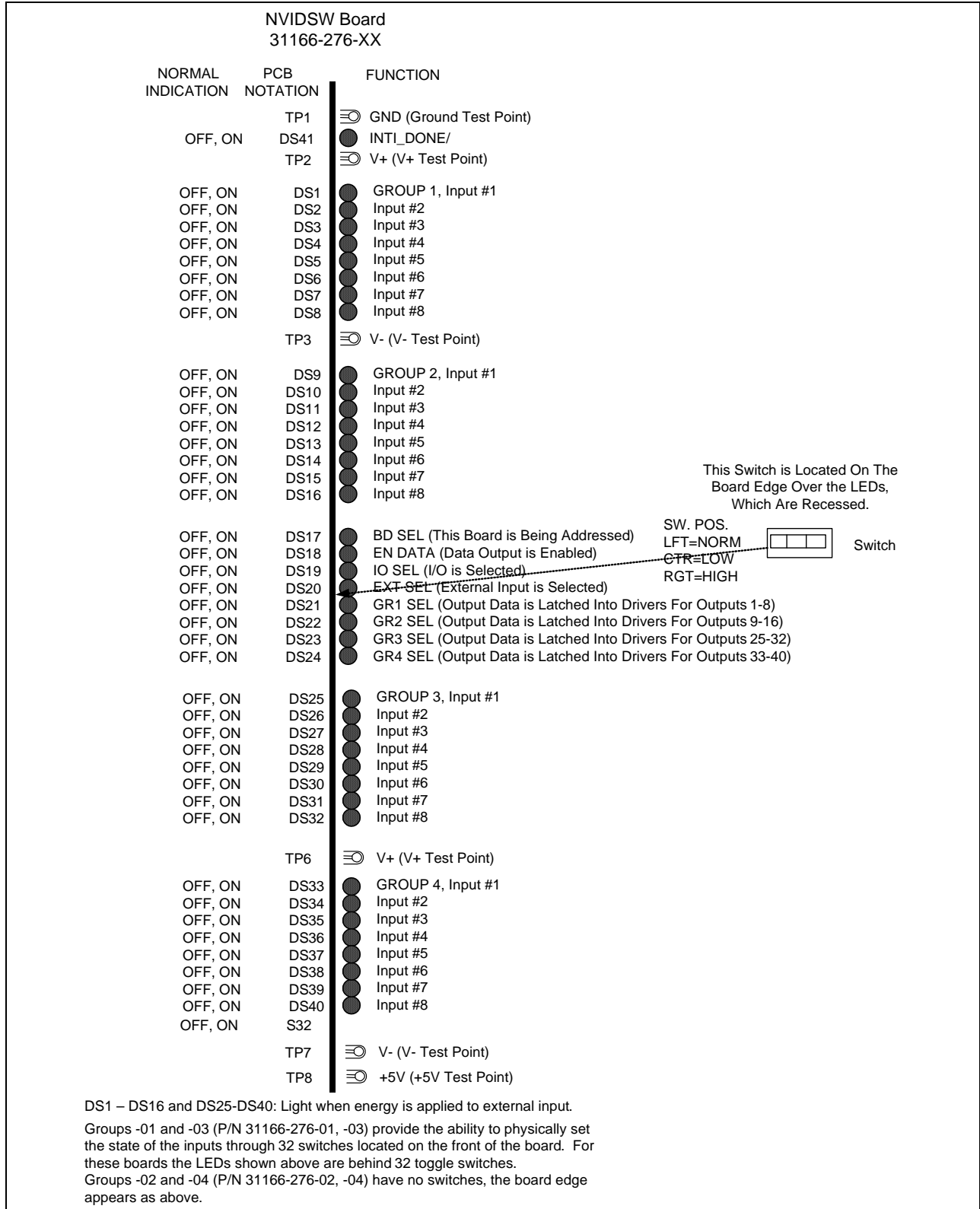


Figure 4–1. NVIDSW Board Edge

4.4. JUMPER SELECTION

The NVIDSW Board is equipped with 8 jumper blocks, which allow the user to make the board non-differential. Using these jumper blocks, the user can either source or sink current for the inputs. The following provides a description of these blocks. Figure 4–2 shows the NVIDSW board jumper and test point locations.

Table 4–1. NVIDSW Board Jumper Selection

Jumper Blocks	
TB1	Input Group 1 (inputs 1-8) Tie-up block
TB2	Input Group 1 (inputs 1-8) Tie-down block
TB3	Input Group 2 (inputs 9-16) Tie-up block
TB4	Input Group 2 (inputs 9-16) Tie-down block
TB5	Input Group 3 (inputs 17-24) Tie-up block
TB6	Input Group 3 (inputs 17-24) Tie-down block
TB7	Input Group 4 (inputs 25-32) Tie-up block
TB8	Input Group 4 (inputs 25-32) Tie-down block

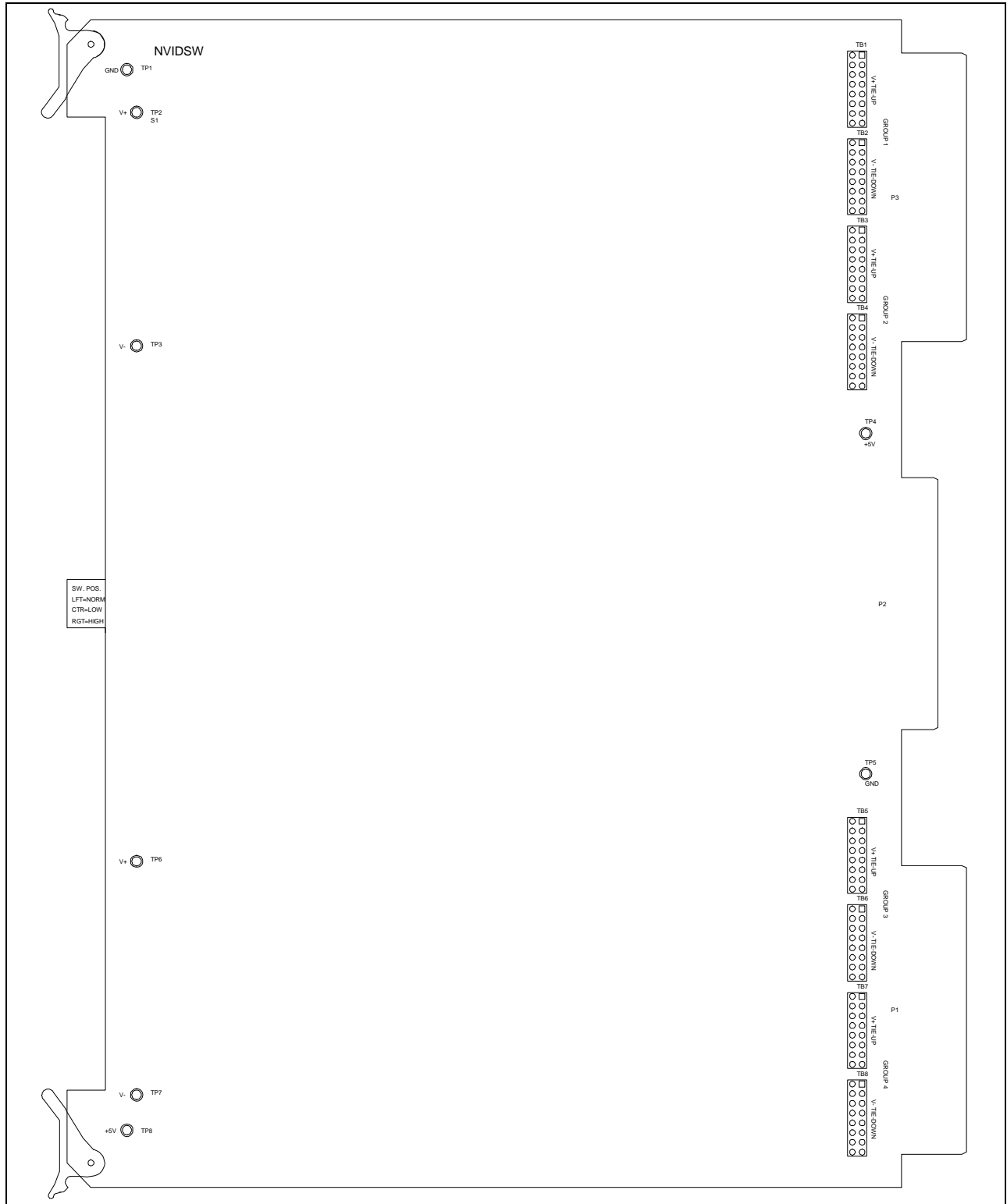


Figure 4–2. NVIDSW Board Jumper and Test Point Locations

4.5. CARD EDGE CONNECTORS

The NVIDSW Board has three card edge connectors:

- P3, the top connector, is a 36-pin connector which contains wiring for input power and inputs 1-16
 - See Table 4–2 for pin configuration details
- P2, the middle connector, is a 50-pin connector which supplies logic power as well as information bits sent to and from the CSEX control board
 - P2-42 through P2-47 are wired in a specific pattern to common P2-48 per the application .lvc CAAPE report for board addressing; the remaining P2 pins are not user configurable
- P1, the lower connector, is a 36-pin connector which contains wiring for input power and inputs 17-32
 - See Table 4–3 for pin configuration details

NOTE

For the user defined inputs and outputs, refer to the .lvc output file generated by the CAAPE program.

Table 4–2. NVIDSW Board 36-pin P3 Connections/

Input	P3-	Name	Function
16	1	Group 2, Bit 7	Low Voltage Pole (GND or V ⁻)
16	2	Group 2, Bit 7	High Voltage Pole (V _{CC} or V ⁺)
15	3	Group 2, Bit 6	Low Voltage Pole (GND or V ⁻)
15	4	Group 2, Bit 6	High Voltage Pole (V _{CC} or V ⁺)
14	5	Group 2, Bit 5	Low Voltage Pole (GND or V ⁻)
14	6	Group 2, Bit 5	High Voltage Pole (V _{CC} or V ⁺)
13	7	Group 2, Bit 4	Low Voltage Pole (GND or V ⁻)
13	8	Group 2, Bit 4	High Voltage Pole (V _{CC} or V ⁺)
12	9	Group 2, Bit 3	Low Voltage Pole (GND or V ⁻)
12	10	Group 2, Bit 3	High Voltage Pole (V _{CC} or V ⁺)
11	11	Group 2, Bit 2	Low Voltage Pole (GND or V ⁻)
11	12	Group 2, Bit 2	High Voltage Pole (V _{CC} or V ⁺)
10	13	Group 2, Bit 1	Low Voltage Pole (GND or V ⁻)
10	14	Group 2, Bit 1	High Voltage Pole (V _{CC} or V ⁺)
9	15	Group 2, Bit 0	Low Voltage Pole (GND or V ⁻)
9	16	Group 2, Bit 0	High Voltage Pole (V _{CC} or V ⁺)
	17	+12V / +24V	Group 2 V _{CC} or V ⁺
	18	COM	Group 2 Ground or V ⁻
8	19	Group 1, Bit 7	Low Voltage Pole (GND or V ⁻)
8	20	Group 1, Bit 7	High Voltage Pole (V _{CC} or V ⁺)
7	21	Group 1, Bit 6	Low Voltage Pole (GND or V ⁻)
7	22	Group 1, Bit 6	High Voltage Pole (V _{CC} or V ⁺)
6	23	Group 1, Bit 5	Low Voltage Pole (GND or V ⁻)
6	24	Group 1, Bit 5	High Voltage Pole (V _{CC} or V ⁺)
5	25	Group 1, Bit 4	Low Voltage Pole (GND or V ⁻)
5	26	Group 1, Bit 4	High Voltage Pole (V _{CC} or V ⁺)
4	27	Group 1, Bit 3	Low Voltage Pole (GND or V ⁻)
4	28	Group 1, Bit 3	High Voltage Pole (V _{CC} or V ⁺)
3	29	Group 1, Bit 2	Low Voltage Pole (GND or V ⁻)
3	30	Group 1, Bit 2	High Voltage Pole (V _{CC} or V ⁺)

Table 4–2. NVIDSW Board 36-pin P3 Connections (Cont.)

Input	P3-	Name	Function
2	31	Group 1, Bit 1	Low Voltage Pole (GND or V ⁻)
2	32	Group 1, Bit 1	High Voltage Pole (V _{CC} or V ⁺)
1	33	Group 1, Bit 0	Low Voltage Pole (GND or V ⁻)
1	34	Group 1, Bit 0	High Voltage Pole (V _{CC} or V ⁺)
	35	+12V / +24V	Group 1 V _{CC} or V ⁺
	36	COM	Group 1 Ground or V ⁻

Table 4–3. NVIDSW Board 36-pin P1 Connections

Input	P1-	Name	Function
32	1	Group 4, Bit 7	Low Voltage Pole (GND or V ⁻)
32	2	Group 4, Bit 7	High Voltage Pole (V _{CC} or V ⁺)
31	3	Group 4, Bit 6	Low Voltage Pole (GND or V ⁻)
31	4	Group 4, Bit 6	High Voltage Pole (V _{CC} or V ⁺)
30	5	Group 4, Bit 5	Low Voltage Pole (GND or V ⁻)
30	6	Group 4, Bit 5	High Voltage Pole (V _{CC} or V ⁺)
29	7	Group 4, Bit 4	Low Voltage Pole (GND or V ⁻)
29	8	Group 4, Bit 4	High Voltage Pole (V _{CC} or V ⁺)
28	9	Group 4, Bit 3	Low Voltage Pole (GND or V ⁻)
28	10	Group 4, Bit 3	High Voltage Pole (V _{CC} or V ⁺)
27	11	Group 4, Bit 2	Low Voltage Pole (GND or V ⁻)
27	12	Group 4, Bit 2	High Voltage Pole (V _{CC} or V ⁺)
26	13	Group 4, Bit 1	Low Voltage Pole (GND or V ⁻)
26	14	Group 4, Bit 1	High Voltage Pole (V _{CC} or V ⁺)
25	15	Group 4, Bit 0	Low Voltage Pole (GND or V ⁻)
25	16	Group 4, Bit 0	High Voltage Pole (V _{CC} or V ⁺)
	17	+12V / +24V	Group 4 V _{CC} or V ⁺
	18	COM	Group 4 Ground or V ⁻
24	19	Group 3, Bit 7	Low Voltage Pole (GND or V ⁻)
24	20	Group 3, Bit 7	High Voltage Pole (V _{CC} or V ⁺)
23	21	Group 3, Bit 6	Low Voltage Pole (GND or V ⁻)
23	22	Group 3, Bit 6	High Voltage Pole (V _{CC} or V ⁺)
22	23	Group 3, Bit 5	Low Voltage Pole (GND or V ⁻)
22	24	Group 3, Bit 5	High Voltage Pole (V _{CC} or V ⁺)
21	25	Group 3, Bit 4	Low Voltage Pole (GND or V ⁻)
21	26	Group 3, Bit 4	High Voltage Pole (V _{CC} or V ⁺)
20	27	Group 3, Bit 3	Low Voltage Pole (GND or V ⁻)
20	28	Group 3, Bit 3	High Voltage Pole (V _{CC} or V ⁺)
19	29	Group 3, Bit 2	Low Voltage Pole (GND or V ⁻)
19	30	Group 3, Bit 2	High Voltage Pole (V _{CC} or V ⁺)

Table 4–3. NVIDSW Board 36-pin P1 Connections (Cont.)

Input	P1-	Name	Function
18	31	Group 3, Bit 1	Low Voltage Pole (GND or V ⁻)
18	32	Group 3, Bit 1	High Voltage Pole (V _{CC} or V ⁺)
17	33	Group 3, Bit 0	Low Voltage Pole (GND or V ⁻)
17	34	Group 3, Bit 0	High Voltage Pole (V _{CC} or V ⁺)
	35	+12V / +24V	Group 3 V _{CC} or V ⁺
	36	COM	Group 3 Ground or V ⁻

4.6. SPECIFICATIONS

Table 4–4. NVIDSW Board Specifications

Specification	31166-276			
	-01	-02	-03	-04
Maximum Number of Boards Per CSEX Subsystem	20			
Board Slots Required	1			
Number of Ports Per Board	32			
Maximum Board Logic Current Supply Draw	200 mA			
Minimum Input Voltage Per Port	9V	9V	18V	18V
Maximum Input Voltage Per Port	18V	18V	33V	33V
Minimum Input Current Per Port to Activate	8.6 ma			
Switches to Force Each Input On/Off	Yes	No	Yes	No

5. SECTION 5 – NVO (NON-VITAL OUTPUT) BOARDS, P/N 59473-785-XX AND 59473-936-XX

5.1. GENERAL

The Non-Vital Output (NVO) Board (P/N 59473-785-XX) and Non-Vital Output AC (NVOAC) Board (P/N 59473-936-XX) provide 32 isolated Non-Vital outputs interfaced through the system Motherboard to the couplers on the back of the module. A CSEX3 Board, employing Non-Vital I/O control software, communicates over the Motherboard bus to the NVO Board. Output states are latched and updated once a second; twice a second if a flashing indication is required.

See Figure A–4 for an NVO board layout drawing and Figure A–5 for an NVOAC board layout drawing.

5.2. OPERATION

Five of the available address bus lines access one of 20 Non-Vital I/O Boards. A logic comparator compares the address on the bus with the slot programmed address; the result is a BOARD SELECT output if they agree.

Figure 5–1 shows a block diagram of the NVO Boards. Operation of the NVO and NVOAC Boards are identical except as noted in this discussion.

NVO outputs are arranged in four groups of 8. Two additional address lines select each of the groups. These outputs, as well as BOARD SELECT, go to a control PROM.

A 32 × 8 bit PROM decodes address and control line information for the latching of the output state. In addition to the above signals, OUTPUT WRITE and address signals provide individual LATCH OUTPUT GROUP signals for each of four output group latches at the PROM output. Other outputs are directed to onboard diagnostic indications so that failures within the address and control logic can be readily observed.

As stated, outputs are latched on an 8-bit basis. A LATCH OUTPUT GROUP signal goes to the clock input of each of four octal latches. An OUTPUT WRITE operation puts the desired 8-bit output port image to the group latch addressed. The latched output states are buffered to drive optical isolators.

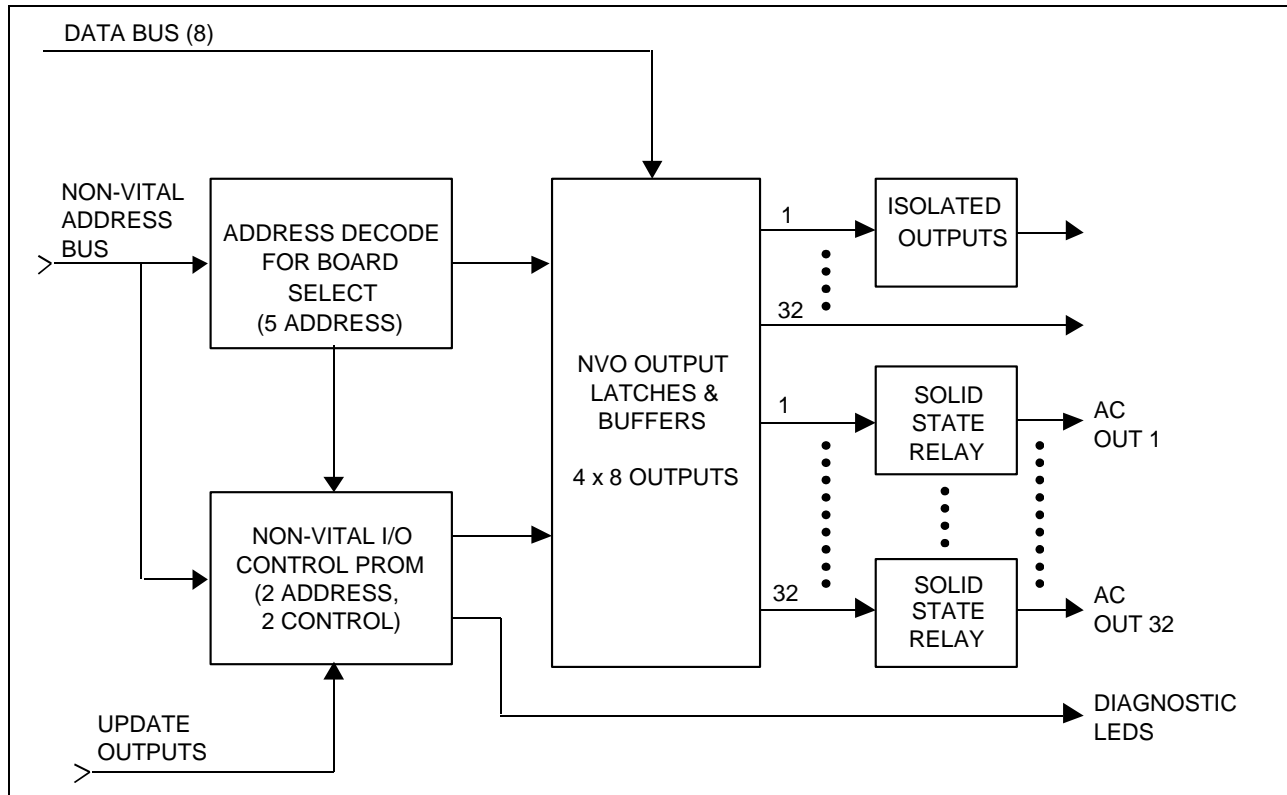


Figure 5–1. NVO Board Block Diagram

5.3. ISOLATED OUTPUTS

Optical isolators separate the power supplies of the 5V logic system and field circuitry. Each of the four groups of 8 outputs possesses a separate power feed and signal return, allowing interface with four distinctly different supplies.

Various board groups have different output voltages (see specifications). Outputs can source up to 250 mA. Secondary transient protection in the form of a suppressor is placed across the output-to-supply common. These suppressors afford protection against induced transients. A series output diode protects and isolates each output as well.

NOTE

The isolation is provided to allow versatility in system application and a degree of noise elimination. The isolation is NOT VITAL. Any field supply used for Vital functions CANNOT be used with this board.

5.4. INDICATIONS

Each output contains an indication representing its state. The LED is connected on the field supply side. These indications along with the output board logic control indications are presented on the front edge of the board. Test points for troubleshooting logic problems are included for several onboard control signals. Figure 5–2 shows the NVO, board indications.

NORMAL INDICATION	PCB NOTATION	FUNCTION
OFF, ON, FLASHING	CR40	● 1 (Output #1)
OFF, ON, FLASHING	CR39	● Output #2
OFF, ON, FLASHING	CR38	● Output #3
OFF, ON, FLASHING	CR37	● Output #4
OFF, ON, FLASHING	CR36	● 5 (Output #5)
OFF, ON, FLASHING	CR35	● Output #6
OFF, ON, FLASHING	CR34	● Output #7
OFF, ON, FLASHING	CR33	● Output #8
OFF, ON, FLASHING	CR32	● 9 (Output #9)
OFF, ON, FLASHING	CR31	● Output #10
OFF, ON, FLASHING	CR30	● Output #11
OFF, ON, FLASHING	CR29	● Output #12
OFF, ON, FLASHING	CR28	● 13 (Output #13)
OFF, ON, FLASHING	CR27	● Output #14
OFF, ON, FLASHING	CR26	● Output #15
OFF, ON, FLASHING	CR25	● Output #16
	TP2	⊕ COM (Common Test Point)
OFF, ON	CR24	● SEL (This Board Is Being Addressed)
OFF, ON	CR23	● DO (CSEX Commands All Outputs Disabled, Usually On Start-up)
OFF, ON	CR22	● IOSEL (An Acceptable Address Occurs)
OFF, ON	CR21	● ESEL (An Acceptable Address Occurs)
OFF, ON	CR20	● LG4 (Output Data Is Latched Into Drivers For Outputs 25-32)
OFF, ON	CR19	● LG3 (Output Data Is Latched Into Drivers For Outputs 17-24)
OFF, ON	CR18	● LG2 (Output Data Is Latched Into Drivers For Outputs 9-16)
OFF, ON	CR17	● LG1 (Output Data Is Latched Into Drivers For Outputs 1-8)
	TP1	⊕ +5V (+5 Volts Test Point)
OFF, ON, FLASHING	CR16	● 17(Output #17)
OFF, ON, FLASHING	CR15	● Output #18
OFF, ON, FLASHING	CR14	● Output #19
OFF, ON, FLASHING	CR13	● Output #20
OFF, ON, FLASHING	CR12	● 21 (Output #21)
OFF, ON, FLASHING	CR11	● Output #22
OFF, ON, FLASHING	CR10	● Output #23
OFF, ON, FLASHING	CR9	● Output #24
OFF, ON, FLASHING	CR8	● 25 (Output #25)
OFF, ON, FLASHING	CR7	● Output #26
OFF, ON, FLASHING	CR6	● Output #27
OFF, ON, FLASHING	CR5	● Output #28
OFF, ON, FLASHING	CR4	● 29 (Output #29)
OFF, ON, FLASHING	CR3	● Output #30
OFF, ON, FLASHING	CR2	● Output #31
OFF, ON, FLASHING	CR1	● Output #32

CR1 - CR20, CR25 - CR40: Light when the output is turned on.

Figure 5–2. NVO Board Edge

NVOAC BOARD 59473-936-XX		
NORMAL INDICATION	PCB NOTATION	FUNCTION
OFF, ON, FLASHING	CR9	● 1 (Output #1)
OFF, ON, FLASHING	CR10	● Output #2
OFF, ON, FLASHING	CR11	● Output #3
OFF, ON, FLASHING	CR12	● Output #4
OFF, ON, FLASHING	CR13	● 5 (Output #5)
OFF, ON, FLASHING	CR14	● Output #6
OFF, ON, FLASHING	CR15	● Output #7
OFF, ON, FLASHING	CR16	● Output #8
OFF, ON, FLASHING	CR17	● 9 (Output #9)
OFF, ON, FLASHING	CR18	● Output #10
OFF, ON, FLASHING	CR19	● Output #11
OFF, ON, FLASHING	CR20	● Output #12
OFF, ON, FLASHING	CR21	● 13 (Output #13)
OFF, ON, FLASHING	CR22	● Output #14
OFF, ON, FLASHING	CR23	● Output #15
OFF, ON, FLASHING	CR24	● Output #16
	TP2	⊕ COM (Common Test Point)
OFF, ON	CR1	● SEL (This Board Is Being Addressed)
OFF, ON	CR2	● DO (CSEX Commands All Outputs Disabled, Usually On Start-up)
OFF, ON	CR3	● IOSEL (An Acceptable Address Occurs)
OFF, ON	CR4	● ESEL (An Acceptable Address Occurs)
OFF, ON	CR5	● LG4 (Output Data Is Latched Into Drivers For Outputs 25-32)
OFF, ON	CR6	● PWR (Output Data Is Latched Into Drivers For Outputs 17-24)
OFF, ON	CR7	● LG3 (Output Data Is Latched Into Drivers For Outputs 9-16)
OFF, ON	CR8	● LG4 (Output Data Is Latched Into Drivers For Outputs 1-8)
	TP1	⊕ +5V (+5 Volts Test Point)
OFF, ON, FLASHING	CR25	● 17 (Output #17)
OFF, ON, FLASHING	CR26	● Output #18
OFF, ON, FLASHING	CR27	● Output #19
OFF, ON, FLASHING	CR28	● Output #20
OFF, ON, FLASHING	CR29	● 21 (Output #21)
OFF, ON, FLASHING	CR30	● Output #22
OFF, ON, FLASHING	CR31	● Output #23
OFF, ON, FLASHING	CR32	● Output #24
OFF, ON, FLASHING	CR33	● 25 (Output #25)
OFF, ON, FLASHING	CR34	● Output #26
OFF, ON, FLASHING	CR35	● Output #27
OFF, ON, FLASHING	CR36	● Output #28
OFF, ON, FLASHING	CR37	● 29 (Output #29)
OFF, ON, FLASHING	CR38	● Output #30
OFF, ON, FLASHING	CR39	● Output #31
OFF, ON, FLASHING	CR40	● Output #32

CR9 - CR40: Light when the output is turned on..

Figure 5–3. NVOAC Board Edge

5.5. TEST POINTS

The test point locations for the NVO board and the NVOAC board are the same, as shown in Figure 5–4.

Table 5–1. NVO and NVOAC Board Test Points

Test Points	
TP1	+5V logic power
TP2	COM, logic common
TP3-1	LATCH.OUT.GRP1
TP3-2	LATCH.OUT.GRP1
TP3-3	BOARD SELECT/
TP3-4	LATCH.OUT.GRP1
TP3-5	LATCH.OUT.GRP1
TP3-6	NVMWR/
TP3-7	EMSEL/
TP3-8	Combination of favorable addresses and EMSEL/ from the non-vital CPU; these additional bits are used to address the board because address range NVA0 -> NVA7 is also used for other functions; HI = this board is disabled, LO = this board is allowed to be enabled

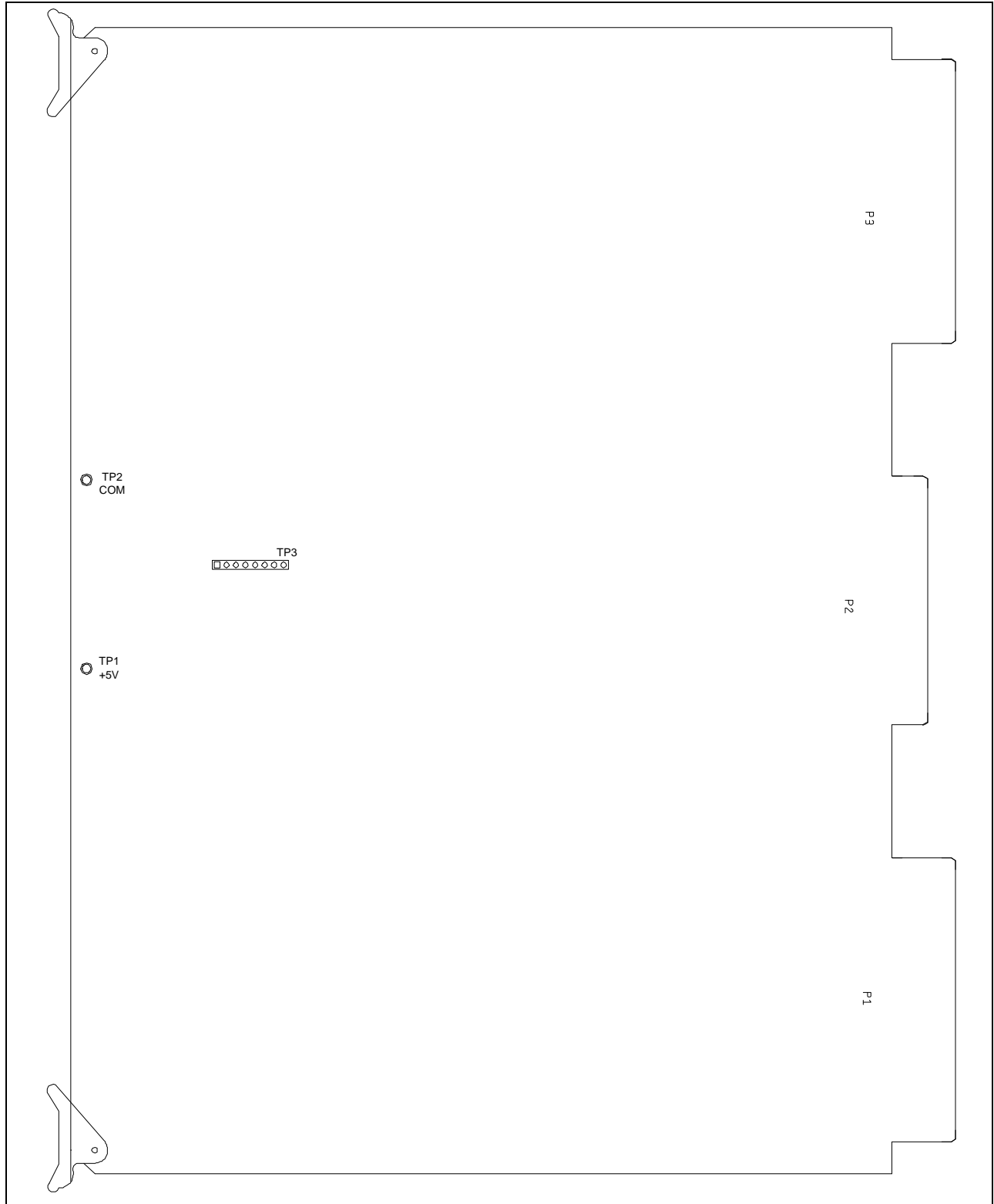


Figure 5–4. NVO Board and NVOAC Board Test Point Locations

5.6. CARD EDGE CONNECTORS

The NVO Board has three card edge connectors:

- P3, the top connector, is a 36-pin connector which contains wiring for outputs 1 – 16 and output common connections
 - See Table 5–2 for 36-pin configuration details
- P2, the middle connector, is a 50-pin connector used for connections to the motherboard which supplies 5 Volt power, control, data and slot addressing signals
 - P2-42 through P2-47 are wired in a specific pattern to common P2-48 per the application .lvc CAAPE report for board addressing; the remaining P2 pins are not user configurable
- P1, the lower connector, is a 36-pin connector which contains wiring for outputs 17 – 32 and output common connections
 - See Table 5–3 for 36-pin configuration details

NOTE

Connector configurations are the same for both the NVO and the NVOAC Boards.

NOTE

For the user defined inputs and outputs, refer to the .lvc output file generated by the CAAPE program.

Table 5–2. NVO Board 36-pin P3 Connections

Output Number	P3-
1	34
2	32
3	30
4	29
5	26
6	25
7	22
8	21
+V (1-8)	35
COM (1-8)	36
9	18
10	17
11	14
12	13
13	10
14	9
15	6
16	5
+V (9-16)	19
COM (9-16)	20

Table 5–3. NVO Board 36-pin P1 Connections

Output Number	P1-
17	34
18	32
19	30
20	29
21	26
22	25
23	22
24	21
+V (17-24)	35
COM (17-24)	36
25	18
26	17
27	14
28	13
29	10
30	9
31	6
32	5
+V (25-32)	19
COM (25-32)	20

5.7. SPECIFICATIONS/ASSEMBLY DIFFERENCES

Table 5–4. NVO Board Specifications

Specification	59473-785				
	-01	-02	-03	-04	-05
Maximum Number of Boards Per CSEX Subsystem	20				
Board Slots Required	1				
Number of Ports Per Board	32				
Maximum Board Logic Current Supply Draw	500 mA				
Minimum Switched Output Supply Voltage	18.0 VDC	9.0 VDC	18.0 VDC	9.0 VDC	4.5 VDC
Maximum Switched Output Supply Voltage	33.0 VDC	18.0 VDC	33.0 VDC	18.0 VDC	14.5 VDC
Maximum Output Current Per Port (Source)	0.25 A	0.25 A	0.25 A	0.25 A	0.25 A
Power On Reset	No	No	Yes	Yes	Yes

Table 5–5. NVOAC Board Specifications

Specification	59473-936	
	-01	-02
Maximum Number of Boards Per CSEX Subsystem	20	
Board Slots Required	1	
Number of PORTS PER BOARD	32	
Maximum Board Logic Current Supply Draw	500 mA	
Minimum Switched Output Supply Voltage	5.0 VAC	
Maximum Switched Output Supply Voltage	250 VAC	
Maximum Output Current Per Port	0.25 A	
Frequency Range	47 - 70 Hz	
Power On Reset	No	Yes

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6. SECTION 6 – NVO-SNK (NON-VITAL OUTPUT SINK) BOARD, P/N 31166-123-XX

6.1. GENERAL

The Non-Vital Sink Output Board provides a VPI II system with 32 Non-Vital, latched, isolated, open drain, current sinking outputs, each capable of driving TTL or CMOS logic inputs.

NOTE

Logic inputs must be provided with an appropriate pull-up resistor.

The outputs are divided into four groups of 8. The outputs are controlled, via the system bus on the system Motherboard, by a CSEX3 board running Non-Vital I/O control software.

See Figure A–6 for a board layout drawing.

6.2. OPERATION

When the CSEX3 board performs an input or output operation, it places an address on certain lines of the system bus. A digital comparator on the output board compares the states of six of the bus address lines with the states of the slot programming inputs, jumpers on the motherboard, of the card slot where the board is located. If the states agree, the operation is intended for this board and a BOARD SELECT signal is generated.

The BOARD SELECT signal is input to a 32 word by 8 bit PROM. The other inputs to the PROM are the write, output select and the two least significant address signals from the system bus. The PROM combines these signals to generate an enable that turns on the line receivers and applies the data from the bus to the data inputs of four output storage registers.

Each of the 8 outputs of each output register is connected to the input of a photo isolator so that there are 32 isolators, one for each output. When the register contains a 0 (zero) in the location represented by the register output, the isolator is turned on. The output transistor of each isolator is configured as an emitter follower which, when turned on, applies the output group positive voltage to the gate of an N-channel MOSFET transistor. The MOSFET is the board output device, which, when the positive voltage is applied to its gate, turns on and connects the corresponding board output to its output group return. The status of each board output is shown by an LED indication connected between the MOSFET drain and its group positive voltage. The LED is lit when the corresponding board output is ON.

The MOSFET output devices are protected from reverse voltages by a Schottky diode in series with the output. They are also protected from overvoltage transients by a Transorb type suppressor between the output and its group return.

Previously, reference was made to a group positive voltage and a group return, plus the arrangement of board outputs into four groups of 8. Each group of 8 outputs is provided with a separate positive supply voltage and corresponding return. The positive voltage supplies the ON bias for the output MOSFETs and the current for the indication LEDs for the outputs of the group. Output load current is sunk to the return by the output MOSFETs. Each of the four groups is electrically separated from the other three groups and all are isolated from the board logic supply.

NOTE

The isolation is provided to allow versatility in system application and a degree of noise elimination. The isolation is NOT VITAL. Any field supply used for Vital functions CANNOT be used with this board.

The board outputs can sink up to 500 mA. Output voltages are typically less than 0.6 volts at a load current of 250 mA over the temperature range from -40 to +70°C. At a load current of 10 mA over the same temperature range the output voltage is typically less than 0.4 volts.

6.3. INDICATIONS

Each output is provided with an LED indication on the edge of the circuit board to indicate the status of that output. Seven other LED indications on the edge of the board show the status of various logic control signals. The status of these signals is latched into a display register each time the CSEX3 board issues a system bus write signal. Figure 6–1 shows the NVO-SNK board indications.

NORMAL INDICATION	PCB NOTATION	FUNCTION
OFF, ON, FLASHING	CR40	● GR1,1 (Output #1)
OFF, ON, FLASHING	CR39	● Output #2
OFF, ON, FLASHING	CR38	● Output #3
OFF, ON, FLASHING	CR37	● Output #4
	CR36	● Output #5
OFF, ON, FLASHING	CR35	● Output #6
OFF, ON, FLASHING	CR34	● Output #7
OFF, ON, FLASHING	CR33	● GR1,8 (Output #8)
OFF, ON, FLASHING	CR32	● GR2,1 (Output #9)
OFF, ON, FLASHING	CR31	● Output #10
OFF, ON, FLASHING	CR30	● Output #11
OFF, ON, FLASHING	CR29	● Output #12
OFF, ON, FLASHING	CR28	● Output #13
OFF, ON, FLASHING	CR27	● Output #14
OFF, ON, FLASHING	CR26	● Output #15
OFF, ON, FLASHING	CR25	● GR2,8 (Output #16)
	TP2	⊖ COM (Common Test Point)
OFF, ON	CR24	● SEL (This Board Is Being Addressed)
OFF, ON	CR23	● DO (CSEX Commands All Outputs Are Disabled, Usually On Start-up)
OFF, ON	CR22	● IOSEL (An Acceptable Address Occurs)
OFF, ON	CR21	● ESEL (An Acceptable Address Occurs)
OFF, ON	CR20	● Output Data Is Latched Into Drivers For Outputs 25-32
OFF, ON	CR19	● Output Data Is Latched Into Drivers For Outputs 17-24
OFF, ON	CR18	● Output Data Is Latched Into Drivers For Outputs 9-16
OFF, ON	CR17	● Output Data Is Latched Into Drivers For Outputs 1-8
	TP1	⊖ +5V (+5 Volts Test Point)
OFF, ON, FLASHING	CR16	● GR3,1 (Output #17)
OFF, ON, FLASHING	CR15	● Output #18
OFF, ON, FLASHING	CR14	● Output #19
OFF, ON, FLASHING	CR13	● Output #20
	CR12	● Output #21
OFF, ON, FLASHING	CR11	● Output #22
OFF, ON, FLASHING	CR10	● Output #23
OFF, ON, FLASHING	CR9	● GR3,8 (Output #24)
OFF, ON, FLASHING	CR8	● GR4,1 (Output #25)
OFF, ON, FLASHING	CR7	● Output #26
OFF, ON, FLASHING	CR6	● Output #27
OFF, ON, FLASHING	CR5	● Output #28
	CR4	● Output #29
OFF, ON, FLASHING	CR3	● Output #30
OFF, ON, FLASHING	CR2	● Output #31
OFF, ON, FLASHING	CR1	● GR4,8 (Output #32)

CR1 - CR20 and CR25 - CR40: Light when the output is turned on.

Figure 6–1. NVO-SNK Board Edge

6.4. TEST POINTS

Figure 6–2 shows the NVO-SNK board test point locations.

Table 6–1. NVO-SNK Board Test Points

Test Points	
TP1	+5V logic power
TP2	COM, logic common
TP3-1	BOARD SELECT/
TP3-2	I/O SELECT/
TP3-3	System Bus WRITE/
TP3-4	LATCH.OUT.GRP1
TP3-5	LATCH.OUT.GRP2
TP3-6	LATCH.OUT.GRP3
TP3-7	LATCH.OUT.GRP4
TP3-8	OUTPUT.EN

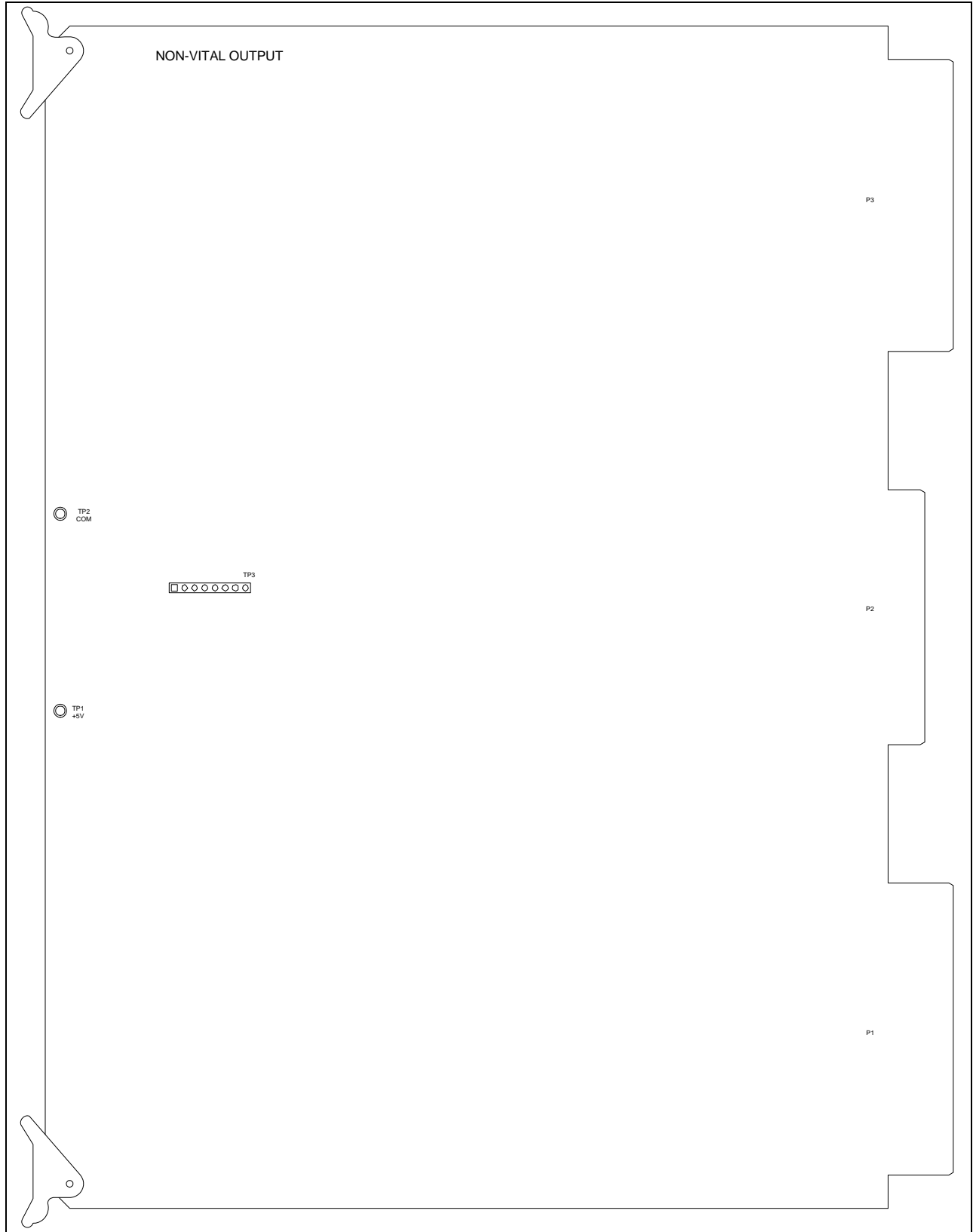


Figure 6-2. NVO-SNK Board Test Point Locations

6.5. CARD EDGE CONNECTORS

The NVO-SNK Board has three card edge connectors:

- P3, the top connector, is a 36-pin connector which contains wiring for outputs 1 – 16 and output common connections
 - See Table 6–2 for 36-pin configuration details
- P2, the middle connector, is a 50-pin connector used for connections to the motherboard which supplies 5 Volt power, control, data and slot addressing signals
 - P2-42 through P2-47 are wired in a specific pattern to common P2-48 per the application .lvc CAAPE report for board addressing; the remaining P2 pins are not user configurable
- P1, the lower connector, is a 36-pin connector which contains wiring for outputs 17 – 32 and output common connections
 - See Table 6–3 for 36-pin configuration details

NOTE

For the user defined inputs and outputs, refer to the .lvc output file generated by the CAAPE program.

Table 6–2. NVO-SNK Board 36-pin P3 Connections

Output Number	P3-
1	34
2	32
3	30
4	29
5	26
6	25
7	22
8	21
+V (1-8)	35
COM (1-8)	36
9	18
10	17
11	14
12	13
13	10
14	9
15	6
16	5
+V (9-16)	19
COM (9-16)	20

Table 6–3. NVO-SNK Board 36-pin P1 Connections

Output Number	P1-
17	34
18	32
19	30
20	29
21	26
22	25
23	22
24	21
+V (17-24)	35
COM (17-24)	36
25	18
26	17
27	14
28	13
29	10
30	9
31	6
32	5
+V (25-32)	19
COM (25-32)	20

6.6. SPECIFICATIONS

Table 6–4. NVO-SNK Board Specifications

Specification	31166-123-01
Maximum Number of Boards Per CSEX Subsystem	20
Board Slots Required	1
Number of PORTS PER BOARD	32
Minimum Switched Output Supply Voltage	4.5 VDC
Maximum Switched Output Supply Voltage	14.5 VDC
Maximum Output Current Per Port	500 mA (sink)
Power On Reset	Yes

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7. SECTION 7 – NVR (NON-VITAL RELAY OUTPUT) BOARD, P/N 31166-238-XX

7.1. GENERAL

The Non-Vital Relay Output (NVR) Board provides 32 Form A non-vital relay contacts (single-pole double-throw contacts with a default state of normally open) interfaced through the system backplane to the couplers on the back of the module. A CSEX3 Board, employing non-vital I/O control software, communicates over the motherboard bus to the NVR Board. Output states are latched and updated once a second; twice a second if a flashing indication is required. Internal circuitry on the NVR Board disables outputs at power-up until a CSEX3 board writes to this board to initialize the outputs.

See Figure A–7 for a board layout drawing.

7.2. OPERATION

Five of the available address bus lines access one of twenty non-vital input/output boards in a system. The NVR Board relays are arranged in four groups of 8. Two address lines allow for selection of the groups (0-3). The slot address, along with seven address lines and two control signals go to an FPGA (Field Programmable Gate Array) on the board. The FPGA processes these signals to determine if the address on the bus matches the slot address of the board. If the two match, the 8 bits on the data bus are stored in the selected register internal to the FPGA. The FPGA also outputs signals to onboard diagnostic indications so that failures within the address and control logic can be readily observed.

Outputs are latched on an 8-bit basis. An output write operation puts the desired 8-bit output port image to the group register addressed. The latched output states are buffered to drive FETs (Field Effect Transistors) which in turn drive the relay coils, enabling the appropriate LED.

When removing or inserting a NVR Board for test or maintenance purposes, follow these important instructions:

1. The 5V power for this board and for the non-vital CPU Board (CSEX3) must be off.
2. The external power supplies for relays and outputs to this board must also be off.

This is important because:

- It helps to avoid damage to both the NVR and other boards.
- It assures an orderly power-up sequence that avoids unwanted output states.

Figure 7–1 shows the NVR board block diagram, a brief summary of the interaction between the FPGA and the various hardware registers (outputs) on the NVR Board.

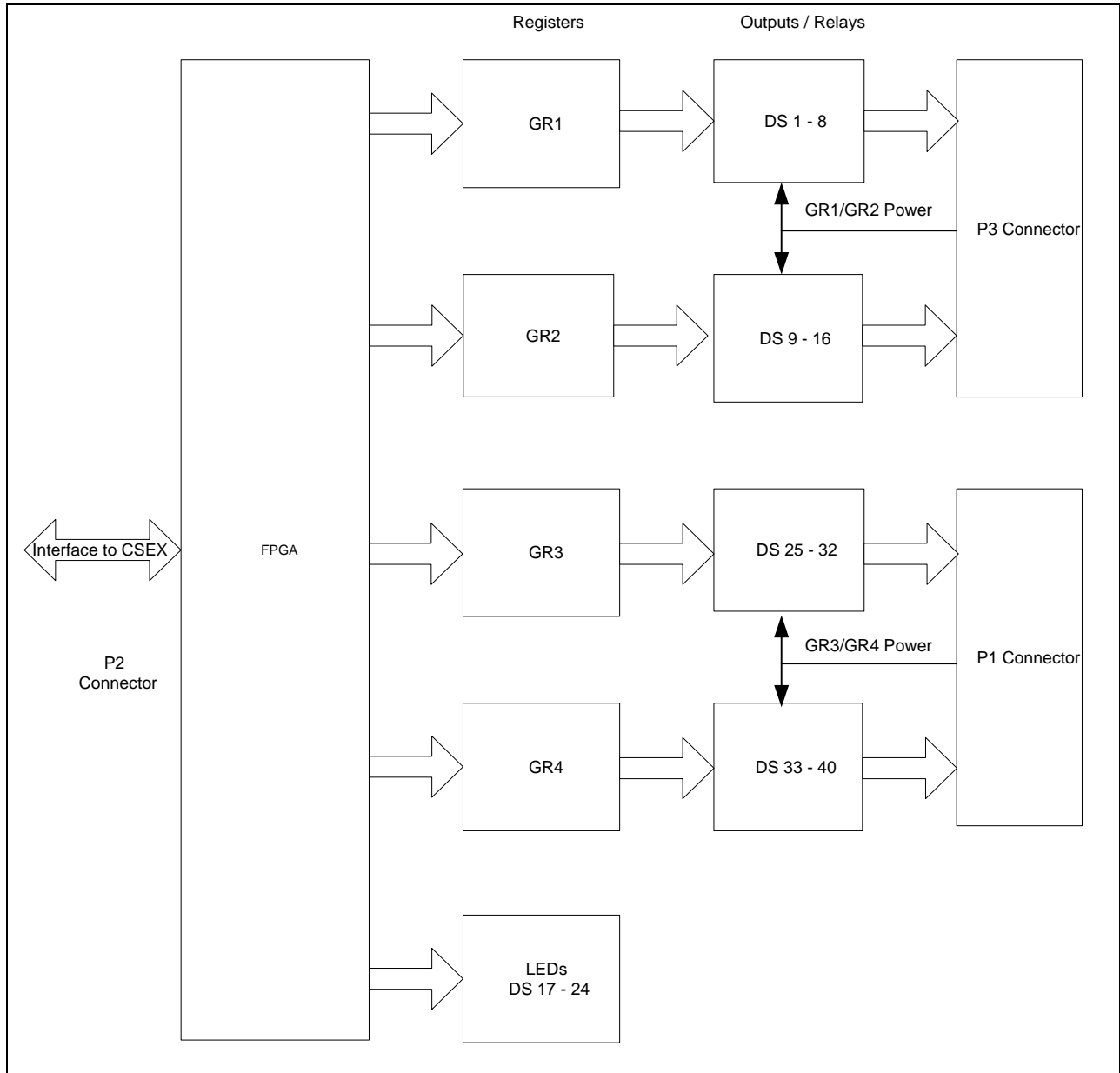


Figure 7–1. NVR Board Block Diagram

7.3. ISOLATED OUTPUTS

Two isolating power supplies for the relay coil drive separate the power supplies of the 5V logic system and field circuitry. There are two separate power feeds. Groups 1 and 2 have one power feed, while groups 3 and 4 have another power feed. Each pair of groups includes 8 relays that run off of one power feed and signal return pair. This configuration allows interface with two distinctly different supplies. The power supplies are truly isolating between the input and output sides.

The NVR Board is functionally equivalent to its NVO (non-vital output) predecessors, except for power requirements and the existence of the Field Programmable Gate Array. The outputs are grouped in four groups with 8 outputs each, as they are in the NVO Board, but the outputs on the P1 and P3 connectors are assigned two pins each, an even and an odd. If the output is currently active, these two pins are connected through the associated relay, allowing current flow.

Two board assembly variations have different voltage ranges for the relay power feeds (see specifications). Secondary transient protection in the form of a suppressor is placed across the relay contacts. These suppressors afford protection against induced transients. Be aware that these relay outputs are not vitally isolated.

NOTE

The isolation is provided to allow versatility in system application and a degree of noise elimination. The isolation is NOT VITAL. Any field supply used for Vital functions CANNOT be used with this board.

7.4. INDICATIONS

Each output contains an LED (Light Emitting Diode) indication representing its state. The LED is controlled by a contact on the relay, and turns on when the relay is closed (which corresponds to an active or true output). These indications, along with the output board control logic indications, are presented on the front edge of the board. Test points for troubleshooting signal problems are included. Figure 7–2 shows the NVR board LED indications, while Table 7–1 describes the test points and their locations.

NVR BOARD 31166-238-XX		
NORMAL INDICATION	PCB NOTATION	FUNCTION
OFF, ON	DS43	● INIT_DONE/
OFF, ON, FLASHING	DS1	● GR1,1(Output #1)
OFF, ON, FLASHING	DS2	● Output #2
OFF, ON, FLASHING	DS3	● Output #3
OFF, ON, FLASHING	DS4	● Output #4
		● Output #5
OFF, ON, FLASHING	DS5	● Output #6
OFF, ON, FLASHING	DS6	● Output #7
OFF, ON, FLASHING	DS7	● GR1,8(Output #8)
OFF, ON, FLASHING	DS8	●
OFF, ON, FLASHING	DS9	● GR2,1 (Output #9)
OFF, ON, FLASHING	DS10	● Output #10
OFF, ON, FLASHING	DS11	● Output #11
OFF, ON, FLASHING	DS12	● Output #12
OFF, ON	DS41	● Group 1 & 2 Power
OFF, ON, FLASHING	DS13	● Output #13
OFF, ON, FLASHING	DS14	● Output #14
OFF, ON, FLASHING	DS15	● Output #15
OFF, ON, FLASHING	DS16	● GR2,8 (Output #16)
OFF, ON	DS17	● BD SEL (This Board Is Being Addressed)
OFF, ON	DS18	● EN DATA \ (Data Output Is Enabled)
OFF, ON	DS19	● IO SEL (I/O Is Selected)
OFF, ON	DS20	● EXT SEL (External Input Is Selected)
OFF, ON	DS21	● GR4 SEL (Output Data Is Latched Into Drivers For Outputs 25-32)
OFF, ON	DS22	● GR3 SEL (Output Data Is Latched Into Drivers For Outputs 17-24)
OFF, ON	DS23	● GR2 SEL (Output Data Is Latched Into Drivers For Outputs 9-16)
OFF, ON	DS24	● GR1 SEL (Output Data Is Latched Into Drivers For Outputs 1-8)
OFF, ON, FLASHING	DS25	● GR3,1 (Output #17)
OFF, ON, FLASHING	DS26	● Output #18
OFF, ON, FLASHING	DS27	● Output #19
OFF, ON, FLASHING	DS28	● Output #20
OFF, ON	DS42	● Group 3 & 4 Power
OFF, ON, FLASHING	DS29	● Output #21
OFF, ON, FLASHING	DS30	● Output #22
OFF, ON, FLASHING	DS31	● Output #23
OFF, ON, FLASHING	DS32	● GR3,8 (Output #24)
OFF, ON, FLASHING	DS33	● GR4,1 (Output #25)
OFF, ON, FLASHING	DS34	● Output #26
OFF, ON, FLASHING	DS35	● Output #27
OFF, ON, FLASHING	DS36	● Output #28
OFF, ON, FLASHING	DS37	● Output #29
OFF, ON, FLASHING	DS38	● Output #30
OFF, ON, FLASHING	DS39	● Output #31
OFF, ON, FLASHING	DS40	● GR4,8 (Output #32)

DS1-DS16 and DS25-DS40: Light when the output is turned on.

Figure 7–2. NVR Board Edge

7.5. TEST POINTS

Figure 7–3 shows the NVR board test point locations.

Table 7–1. NVR Board Test Points

Test Point	Function
TP1	+5V for relay power group A (near PS1)
TP2	+5V logic power (near PS1)
TP3	GND (near PS2)
TP4	+5V for relay power group B (near PS2)
TP5	GND (near FPGA)
TP6	+5V logic power (near FPGA)

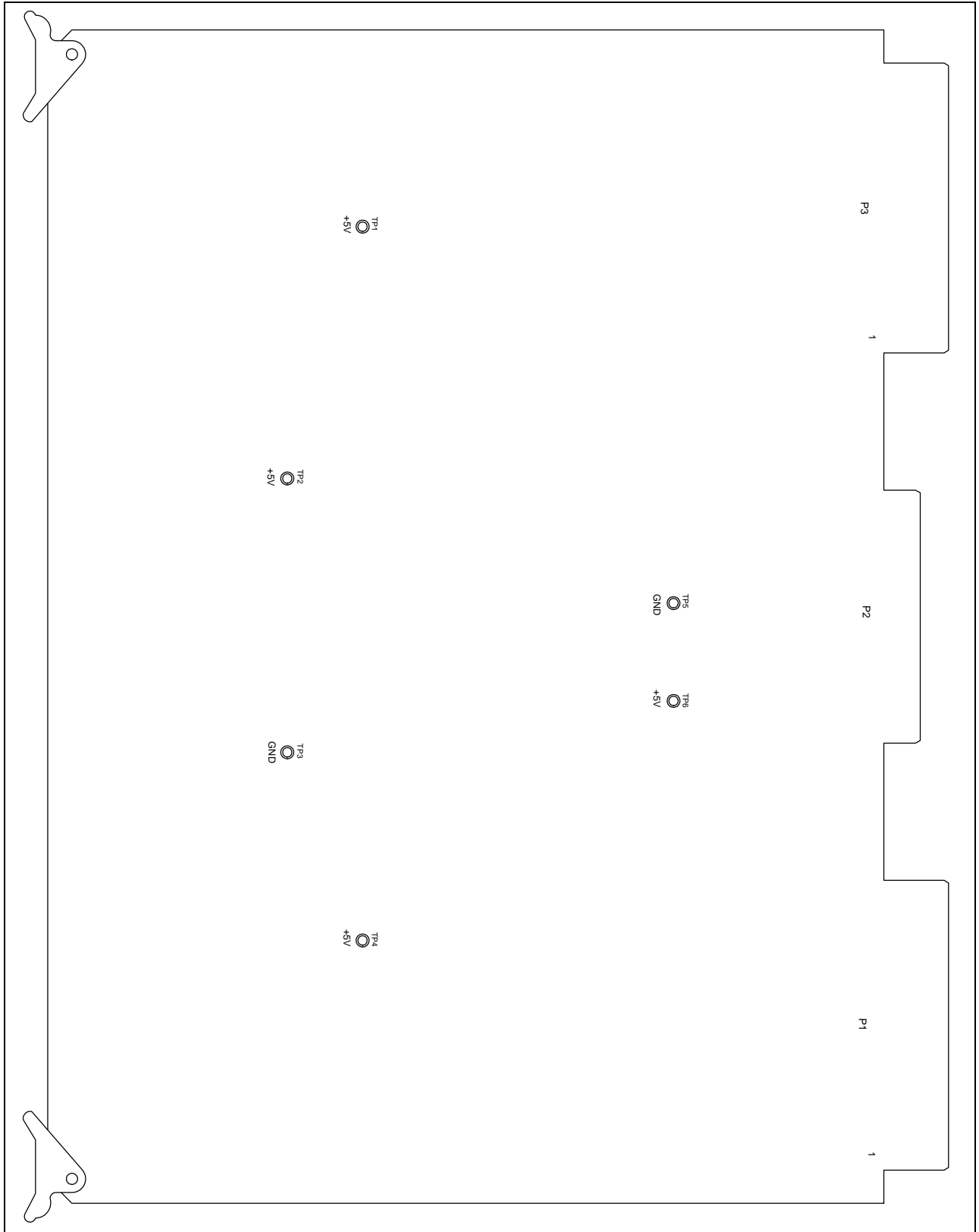


Figure 7-3. NVR Board Test Point Locations

7.6. CARD EDGE CONNECTORS

The NVR Board has three card edge connectors:

- P3, the top connector, is a 36-pin connector which contains wiring for outputs 1 – 16 and power supply connections
 - See Table 7–2 for 36-pin configuration details
- P2, the middle connector, is a 50-pin connector used for communication with a CSEX board, and also to supply +5V logic power
 - P2-42 through P2-47 are wired in a specific pattern to common P2-48 per the application .lvc CAAPE report for board addressing; the remaining P2 pins are not user configurable
- P1, the lower connector, is a 36-pin connector which contains wiring for outputs 17 – 32 and power supply connections
 - See Table 7–3 for 36-pin configuration details

NOTE

For the user defined inputs and outputs, refer to the .lvc output file generated by the CAAPE program.

Table 7–2. NVR Board 36-pin P3 Connections

Output	Name	State	Connection
COM	COM		P3-36 Ground
+12V / + 24V	+12V / + 24V		P3-35 12V power supply (31166-238-01) 24V power supply (31166-238-02)
1	Group 1, Bit 0	ON OFF	P3-33 Connected to P3-34 P3-33 Not Connected to P3-34
2	Group 1, Bit 1	ON OFF	P3-31 Connected to P3-32 P3-31 Not Connected to P3-32
3	Group 1, Bit 2	ON OFF	P3-29 Connected to P3-30 P3-29 Not Connected to P3-30
4	Group 1, Bit 3	ON OFF	P3-27 Connected to P3-28 P3-27 Not Connected to P3-28
5	Group 1, Bit 4	ON OFF	P3-25 Connected to P3-26 P3-25 Not Connected to P3-26
6	Group 1, Bit 5	ON OFF	P3-23 Connected to P3-24 P3-23 Not Connected to P3-24
7	Group 1, Bit 6	ON OFF	P3-21 Connected to P3-22 P3-21 Not Connected to P3-22
8	Group 1, Bit 7	ON OFF	P3-19 Connected to P3-20 P3-19 Not Connected to P3-20
COM	COM		P3-18 Ground
+12V / + 24V	+12V / + 24V		P3-17 12V power supply (31166-238-01) 24V power supply (31166-238-02)
9	Group 2, Bit 0	ON OFF	P3-15 Connected to P3-16 P3-15 Not Connected to P3-16
10	Group 2, Bit 1	ON OFF	P3-13 Connected to P3-14 P3-13 Not Connected to P3-14

Table 7–2. NVR Board 36-pin P3 Connections (Cont.)

Output	Name	State	Connection
11	Group 2, Bit 2	ON OFF	P3-11 Connected to P3-12 P3-11 Not Connected to P3-12
12	Group 2, Bit 3	ON OFF	P3-9 Connected to P3-10 P3-9 Not Connected to P3-10
13	Group 2, Bit 4	ON OFF	P3-7 Connected to P3-8 P3-7 Not Connected to P3-8
14	Group 2, Bit 5	ON OFF	P3-5 Connected to P3-6 P3-5 Not Connected to P3-6
15	Group 2, Bit 6	ON OFF	P3-3 Connected to P3-4 P3-3 Not Connected to P3-4
16	Group 2, Bit 7	ON OFF	P3-1 Connected to P3-2 P3- Not Connected to P3-2

Table 7–3. NVR Board 36-pin P1 Connections

Output	Name	State	Connection
COM	COM		P1-36 Ground
+12V / + 24V	+12V / + 24V		P1-35 12V power supply (31166-238-01) 24V power supply (31166-238-02)
17	Group 3, Bit 1	ON OFF	P1-31 Connected to P1-32 P1-31 Not Connected to P1-32
18	Group 3, Bit 0	ON OFF	P1-33 Connected to P1-34 P1-33 Not Connected to P3-34
19	Group 3, Bit 3	ON OFF	P1-27 Connected to P1-28 P1-27 Not Connected to P1-28
20	Group 3, Bit 2	ON OFF	P1-29 Connected to P1-30 P1-29 Not Connected to P1-30
21	Group 3, Bit 5	ON OFF	P1-23 Connected to P1-24 P1-23 Not Connected to P1-24
22	Group 3, Bit 4	ON OFF	P1-25 Connected to P1-26 P1-25 Not Connected to P1-26
23	Group 3, Bit 7	ON OFF	P1-19 Connected to P1-20 P1-19 Not Connected to P1-20
24	Group 3, Bit 6	ON OFF	P1-21 Connected to P1-22 P1-21 Not Connected to P1-22
COM	COM		P1-18 Ground
+12V / + 24V	+12V / + 24V		P1-17 12V power supply (31166-238-01) 24V power supply (31166-238-02)
25	Group 4, Bit 0	ON OFF	P1-15 Connected to P1-16 P1-15 Not Connected to P1-16
26	Group 4, Bit 1	ON OFF	P1-13 Connected to P1-14 P1-13 Not Connected to P1-14

Table 7–3. NVR Board 36-pin P1 Connections (Cont.)

Output	Name	State	Connection
27	Group 4, Bit 2	ON OFF	P1-11 Connected to P1-12 P1-11 Not Connected to P1-12
28	Group 4, Bit 3	ON OFF	P1-9 Connected to P1-10 P1-9 Not Connected to P1-10
29	Group 4, Bit 4	ON OFF	P1-7 Connected to P1-8 P1-7 Not Connected to P1-8
30	Group 4, Bit 5	ON OFF	P1-5 Connected to P1-6 P1-5 Not Connected to P1-6
31	Group 4, Bit 6	ON OFF	P1-3 Connected to P1-4 P1-3 Not Connected to P1-4
32	Group 4, Bit 7	ON OFF	P1-2 Connected to P1-1 P1-2 Not Connected to P1-1

7.7. SPECIFICATIONS

Table 7–4. NVR Board Specifications

Specification	31166-238	
	-01	-02
Maximum Number of Boards Per CSEX Subsystem	20	
Board Slots Required	1	
Number of Ports Per Board	32	
Maximum Board Logic Current Supply Draw	500 mA	
Minimum Switched Coil Energy Supply Voltage	9.0 VDC	18.0 VDC
Maximum Switched Coil Energy Supply Voltage	18.0 VDC	35.0 VDC
Maximum Current Per Relay Contact Port	1 A	
Maximum Contact Power Rating	30 W / 62.5 VA	
Maximum Contact Voltage	34.8 VDC *	
Power On Reset	Yes	

* This is a limit imposed by the 1.5KE43CA bi-directional suppressor. Actual contact rating is 100 VDC or 125 VAC

7.8. ASSEMBLY DIFFERENCES

There are two versions of the NVR Board:

- 31166-238-01 For use with 9V to 18V power supply for relays
- 31166-238-02 For use with 18V to 35V power supply for relays

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8. SECTION 8 – NVTWC-FSK (NON-VITAL TWC FREQUENCY SHIFT KEYING) BOARD, P/N 31166-119-XX

8.1. GENERAL

The Non-Vital TWC Frequency Shift Keying (NVTWC-FSK) Board provides true Frequency Shift Keying TWC. The incoming TWC messages are keyed such that the logic 1 and logic 0 frequencies are based symmetrically around some base frequency (example: 9650 ± 150 Hz). This board uses 4 Phase Lock Loops (1 per channel) to decode the incoming signals. The output of the phase lock loops are then reformatted so that they can then be sent to the CSEX3 Board.

See Figure A–8 for a board layout drawing.

8.2. OPERATION

Menu-driven board diagnostics can be accessed with a VT100 terminal or equivalent. The diagnostics allows the user to view incoming receive messages, transmit messages and to view commands to and from the CSEX3 Board. In addition, a complete self-test of the board is available via a diagnostic loop back cable. Additional information for a specific application can be found in Alstom specific system manuals.

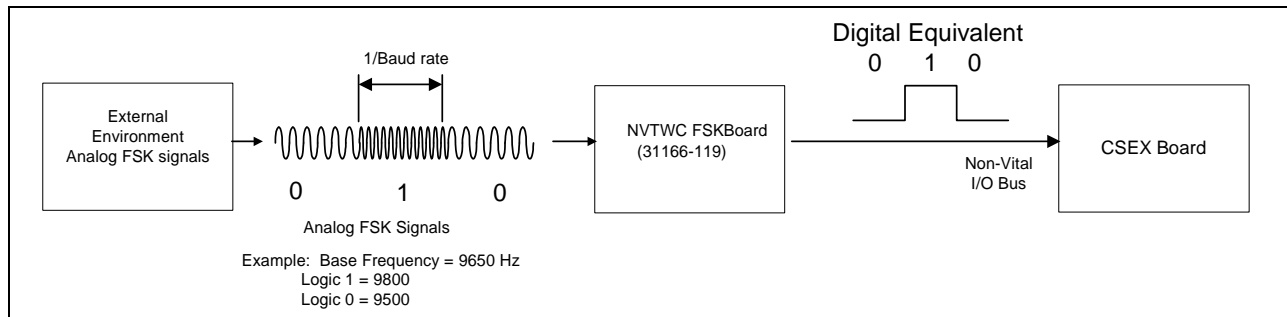


Figure 8–1. NVTWC-FSK Board Subsystem Block Diagram

8.3. INDICATIONS

Figure 8–2 shows the NVTWC-FSK board LED indications.
























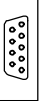


NORMAL INDICATION	PCB NOTATION	FUNCTION
	S1	 RESET (Reset Switch)
	E1	 RCV IN 4 (Channel 4 Receive Data Test Point)
	E2	 DEMOD DAT 4 (Channel 4 Demodulated Data Test Point)
	E3	 DEMOD DAT 3 (Channel 3 Demodulated Data Test Point)
	E4	 RCV IN 3 (Channel 3 Receive Data Test Point)
	E1	 DEMOD DAT 2 (Channel 2 Demodulated Data Test Point)
	E2	 RCV IN 2 (Channel 2 Receive Data Test Point)
	E3	 DEMOD DAT 1 (Channel 1 Demodulated Data Test Point)
	E4	 RCV IN 1 (Channel 1 Receive Data Test Point)
ON, OFF	DS1	 RXON (Channel 4 Receive)
ON, OFF	DS2	 Channel 3 Receive
ON, OFF	DS3	 Channel 2 Receive
ON, OFF	DS4	 Channel 1 Receive
ON, OFF	DS5	 TEST (Channel 4 Receive Enable)
ON, OFF	DS6	 Channel 3 Receive Enable
ON, OFF	DS7	 Channel 2 Receive Enable
ON, OFF	DS8	 Channel 1 Receive Enable
ON, OFF	DS9	 TXID (Channel 4 Transmit)
ON, OFF	DS10	 Channel 3 Transmit
ON, OFF	DS11	 Channel 2 Transmit
ON, OFF	DS12	 Channel 1 Transmit
ON, OFF	DS13	 BD SEL (Board Select)
ON, OFF	DS14	 RESET (Board Reset)
	J2	 (MAC Port)
	E9	 +5V (+5 Volts Test Point)
	E10	 COM (Common Test Point)

Figure 8–2. NVTWC-FSK Board Edge

8.4. TEST POINTS

Figure 8–3 shows the NVTWC-FSK board port, switch, and test point locations.

Table 8–1. NVTWC-FSK Board Test Points

Test Point	Function
E1	RCV_IN_4
E2	DEMOD_DATA_4
E3	DEMOD_DATA_3
E4	RCV_IN_3
E5	DEMOD_DATA_2
E6	RCV_IN_2
E7	DEMOD_DATA_1
E8	RCV_IN_1
E9	+5V logic power
E10	COM, logic common
TP1	RXSPACE3
TP2	RXLOCK3
TP3	RXMARK3
TP4	RXSPACE4
TP5	RXLOCK4
TP6	RXMARK4
TP7	RXSPACE1
TP8	RXLOCK1
TP9	RXMARK1
TP10	RXSPACE2
TP11	RXLOCK2
TP12	RXMARK2

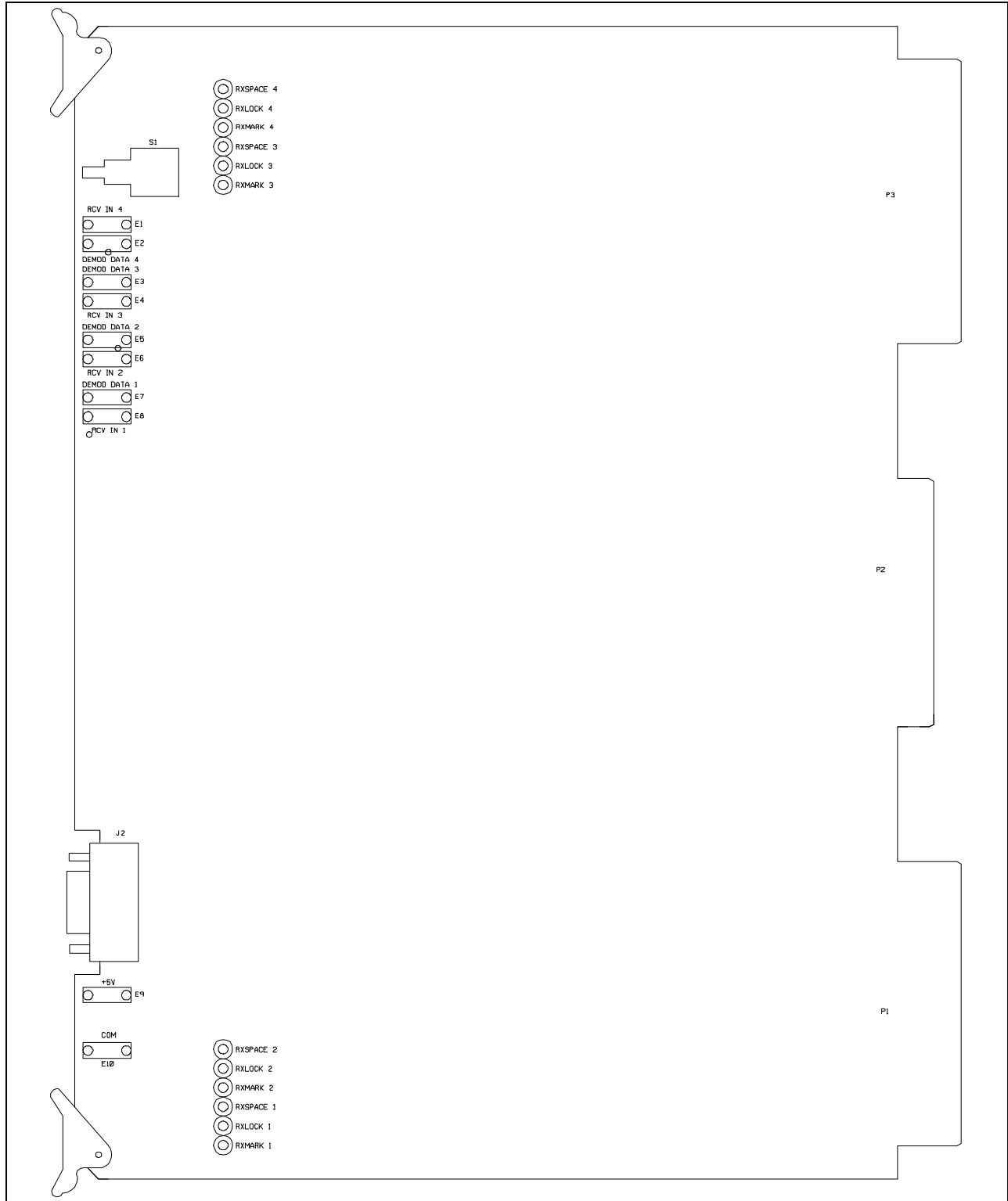


Figure 8-3. NVTWC-FSK Board Port, Switch, Test Point Locations

8.5. CARD EDGE CONNECTORS

The NVTWC-FSK Board has three card edge connectors:

- P3, the top connector, is a 36-pin connector which contains wiring for Channels 3 and 4 and power supply connections
 - See Table 8–2 for 36-pin configuration details
- P2, the middle connector, is a 50-pin connector used for communication with a CSEX board, and also to supply +5V logic power
 - P2-43 through P2-47 are wired in a specific pattern to common P2-48 per the application .lvc CAAPE report for board addressing; the remaining P2 pins are not user configurable
- P1, the lower connector, is a 36-pin connector which contains wiring for Channels 1 and 2 and power supply connections
 - See Table 8–3 for 36-pin configuration details

NOTE

For the user defined inputs and outputs, refer to the .lvc output file generated by the CAAPE program.

Table 8–2. NVTWC-FSK Board 36-pin P3 Connections

P3-	Name	Function
1	TXIDD3+	Channel 3 TX data source
2	COM	Channel 3 TX common
3	TXIDON3+	Channel 3 TX enable source
4	COM	Channel 3 TX common
5 - 8		(not used)
9	RX_3+	Channel 3 RX data drive
10	RX_3-	Channel 3 RX data return
11		(not used)
12		(not used)
13	RX_4+	Channel 4 RX data drive
14	RX_4-	Channel 4 RX data return
15	TXIDD4+	Channel 4 TX data source
16	COM	Channel 4 TX common
17	TXIDON4+	Channel 4 TX enable source
18	COM	Channel 4 TX common
19 - 22		(not used)
23	TXDEF0	Channel 3/4 default transmit
24	COM	5V common
25 - 36		(not used)

Table 8–3. NVTWC-FSK Board 36-pin P1 Connections

P1-	Name	Function
1 - 12		(not used)
13	TXDEF1	Channel 1/2 default transmit
14	COM	+5V common
15	TXIDD1+	Channel 1 TX data source
16	COM	Channel 1 TX common
17	TXIDON1+	Channel 1 TX enable source
18	COM	Channel 1 TX common
19 - 22		(not used)
23	RX_1+	Channel 1 RX data drive
24	RX_1–	Channel 1 RX data return
25		(not used)
26		(not used)
27	RX_2+	Channel 2 RX data drive
28	RX_2–	Channel 2 RX data return
29	TXIDD2+	Channel 2 TX data source
30	COM	Channel 2 TX common
31	TXIDON2+	Channel 2 TX enable source
32	COM	Channel 2 TX common
33 - 36		(not used)

8.6. SPECIFICATIONS/ASSEMBLY DIFFERENCES

Table 8–4. NVTWC-FSK Board Specifications

Specification	31166-119				
	-02	-03	-04	-05	-06
Maximum Number of Output Boards Per VPI II System	8				
Board Slots Required	1				
Maximum Board Logic Current Supply Draw	350 mA				
Number of Detection Channels	4				
Maximum Baud Rate	110	110	100	4800	100
Maximum Detection Frequency	10 kHz	10 kHz	10 kHz	65 kHz	10 kHz
Software	4 Channel TWC Receive only (40025-238)	4 Channel TWC Transmit/Receive (40025-242)	4 Channel TWC Transmit/Receive (40025-284)	4 Channel TWC Transmit/Receive (40025-289)	4 Channel TWC Transmit/Receive (40025-295)

9. SECTION 9 – NVTWC-MOD (NON-VITAL TWC MODEM) BOARD, P/N 31166-099-XX

9.1. GENERAL

This board is used to extract Analog Frequency information into digital format and then pass it on to a CSEX3 board as illustrated in Figure 9–1. In general TWC use, there are two different frequencies representing a logical 1 and a logical 0 for a given communication link. These two frequencies must both be below 10 kHz. There are four channels on the board, each one capable of recognizing one distinct frequency via a very selective bandpass filter. In some applications, it may be desirable to use two channels for each communications link (one to detect the logical 1 frequency and one to detect the logic 0 frequency). In other applications, it may be acceptable to simply detect the logical 1 frequency and assume logical 0 otherwise. This board can be configured (by Alstom) to meet a variety of applications. An onboard microprocessor and FPGAs (programmable hardware) allow a considerable degree of flexibility.

See Figure A–9 for a board layout drawing.

9.2. OPERATION

Menu driven board diagnostics can be accessed with a VT100 terminal or equivalent. The diagnostics allows the user to view incoming receive messages, transmit messages and to view commands to and from the CSEX3 Board. In addition, a complete self-test of the board is available via a diagnostic loop back cable. Additional information for a specific application can be found in Alstom specific system manuals.

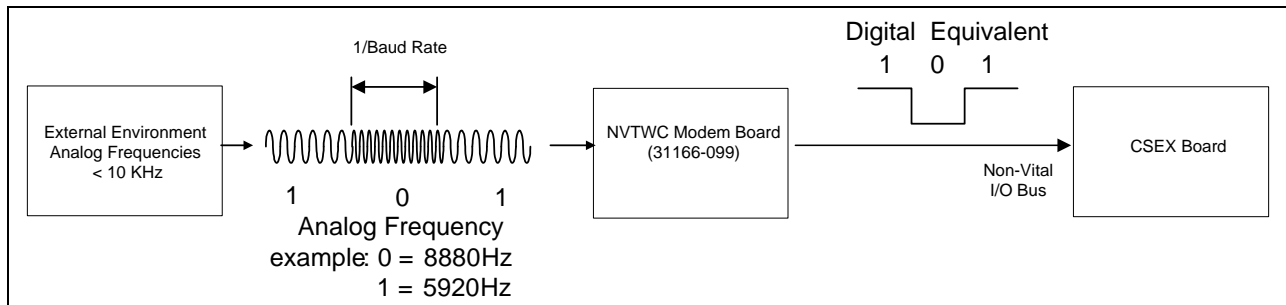


Figure 9–1. NVTWC-MOD Board Subsystem Block Diagram

9.3. INDICATIONS

Figure 9–2 shows the NVTWC-MOD board LED indications.



























NVTWC-MOD BOARD 31166-099-XX		
NORMAL INDICATION	PCB NOTATION	FUNCTION
	S1	 RESET (Reset Switch)
ON, OFF	DS1	 (Channel #4 TX Data)
ON, OFF	DS2	 (Channel #4 RX Data)
ON, OFF	DS3	 (Channel #4 PS Data)
ON, OFF	DS4	 (Channel #4 18Hz Bit Clock)
ON, OFF	DS5	 (Channel #4 3Hz Track Sync)
ON, OFF	DS6	 (Channel #3 TX Data)
ON, OFF	DS7	 (Channel #3 RX Data)
ON, OFF	DS8	 (Channel #3 PS Data)
ON, OFF	DS9	 (Channel #3 18Hz Bit Clock)
ON, OFF	DS10	 (Channel #3 3Hz Track Sync)
ON, OFF	DS11	 (Board Select)
ON, OFF	DS12	 (Channel #2 TX Data)
ON, OFF	DS13	 (Channel #2 RX Data)
ON, OFF	DS14	 (Channel #2 PS Data)
ON, OFF	DS15	 (Channel #2 18Hz Bit Clock)
ON, OFF	DS16	 (Channel #2 3Hz Track Sync)
ON, OFF	DS17	 (Channel #1 TX Data)
ON, OFF	DS18	 (Channel #1 RX Data)
ON, OFF	DS19	 (Channel #1 PS Data)
ON, OFF	DS20	 (Channel #1 18Hz Bit Clock)
ON, OFF	DS21	 (Channel #1 3Hz Track Sync)
OFF	DS22	 (Reset)
	J2	 (MAC Port)
	E1	 COM (Common Test Point)
	E2	 +5V (+5 Volts Test Point)

Figure 9–2. NVTWC-MOD Board Edge

9.4. TEST POINTS

Figure 9–3 shows the NVTWC-MOD board port, switch, and test point locations.

Table 9–1. NVTWC-MOD Board Test Points

Test Point	Function
E1	+5V logic power
E2	COM, logic common
TP5-TP1	RX1
TP6-TP2	RX2
TP7-TP3	RX3
TP8-TP4	RX4

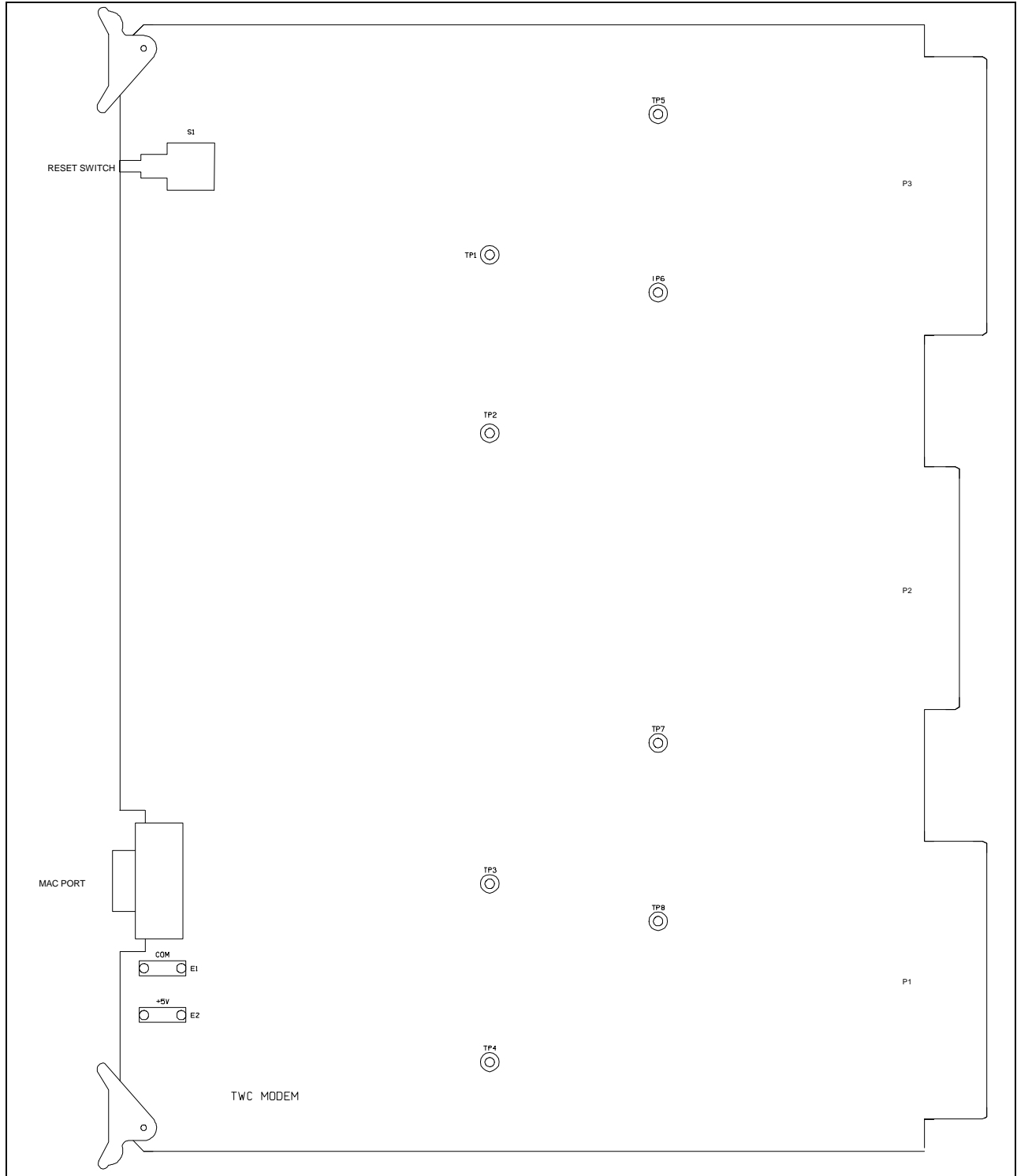


Figure 9-3. NVTWC-MOD Board Port, Switch, Test Point Locations

9.5. CARD EDGE CONNECTORS

The NVTWC-MOD Board has three card edge connectors:

- P3, the top connector, is a 36-pin connector which contains wiring for Channels 3 and 4 and power supply connections
 - See Table 9–2 for 36-pin configuration details
- P2, the middle connector, is a 50-pin connector used for communication with a CSEX board, and also to supply +5V logic power
 - P2-42 through P2-47 are wired in a specific pattern to common P2-48 per the application .lvc CAAPE report for board addressing; the remaining P2 pins are not user configurable
- P1, the lower connector, is a 36-pin connector which contains wiring for Channels 1 and 2 and power supply connections
 - See Table 9–3 for 36-pin configuration details

NOTE

For the user defined inputs and outputs, refer to the .lvc output file generated by the CAAPE program.

Table 9–2. NVTWC-MOD Board 36-pin P3 Connections

P3-	Name	Function
1	TXIDD3+	Channel 3 TX data source
2	COM	Channel 3 TX common
3	TXIDON3+	Channel 3 TX enable source
4	COM	Channel 3 TX common
5	TXPSON3+	Channel 3 PS enable source
6	COM	Channel 3 PS common
7	TXPSD3+	Channel 3 PS data source
8	COM	Channel 3 PS common
9	RXID3L+	Channel 3 RX data low-level drive
10	RXID3-	Channel 3 RX data return
11	RXID3H+	Channel 3 RX data high-level drive
12	RXID4H+	Channel 4 RX data high-level drive
13	RXID4L+	Channel 4 RX data low-level drive
14	RXID4-	Channel 4 RX data return
15	TXIDD4+	Channel 4 TX data source
16	COM	Channel 4 TX common
17	TXIDON4+	Channel 4 TX enable source
18	COM	Channel 4 TX common
19	TXPSON4+	Channel 4 PS enable source
20	COM	Channel 4 PS common
21	TXPSD4+	Channel 4 PS data source
22	COM	Channel 4 PS common
23	TXDEF3/4	Channel 3/4 default transmit
24	COM	+5V common
25	SYNO7+	3Hz Track sync. 7 drive
26	SYNO7-	3Hz Track sync. 7 return
27	SYNO8+	3Hz Track sync. 8 drive
28	SYNO8-	3Hz Track sync. 8 return
29	SYNO9+	3Hz Track sync. 9 drive
30	SYNO9-	3Hz Track sync. 9 return

Table 9–2. NVTWC-MOD Board 36-pin P3 Connections (Cont.)

P3-	Name	Function
31	SYNO10+	3Hz Track sync. 10 drive
32	SYNO10-	3Hz Track sync. 10 return
33	SYNO11+	3Hz Track sync. 11 drive
34	SYNO11-	3Hz Track sync. 11 return
35	SYNO12+	3Hz Track sync. 12 drive
36	SYNO12-	3Hz Track sync. 12 return

Table 9–3. NVTWC-MOD Board 36-pin P1 Connections

P1-	Name	Function
1	SYNO1+	3Hz Track sync. 1 drive
2	SYNO1-	3Hz Track sync. 1 return
3	SYNO2+	3Hz Track sync. 2 drive
4	SYNO2-	3Hz Track sync. 2 return
5	SYNO3+	3Hz Track sync. 3 drive
6	SYNO3-	3Hz Track sync. 3 return
7	SYNO4+	3Hz Track sync. 4 drive
8	SYNO4-	3Hz Track sync. 4 return
9	SYNO5+	3Hz Track sync. 5 drive
10	SYNO5-	3Hz Track sync. 5 return
11	SYNO6+	3Hz Track sync. 6 drive
12	SYNO6-	3Hz Track sync. 6 return
13	TXDEF1/2	Channel 1/2 default transmit
14	COM	+5V common
15	TXIDD1+	Channel 1 TX data source
16	COM	Channel 1 TX common
17	TXIDON1+	Channel 1 TX enable source
18	COM	Channel 1 TX common
19	TXPSON1+	Channel 1 PS enable source
20	COM	Channel 1 PS common
21	TXPSD1+	Channel 1 PS data source
22	COM	Channel 1 PS common
23	RXID1L+	Channel 1 RX data low-level drive
24	RXID1-	Channel 1 RX data return
25	RXID1H+	Channel 1 RX data high-level drive
26	RXID2H+	Channel 2 RX data high-level drive
27	RXID2L+	Channel 2 RX data low-level drive
28	RXID2-	Channel 2 RX data return
29	TXIDD2+	Channel 2 TX data source
30	COM	Channel 2 TX common

Table 9–3. NVTWC-MOD Board 36-pin P1 Connections (Cont.)

P1-	Name	Function
31	TXIDON2+	Channel 2 TX enable source
32	COM	Channel 2 TX common
33	TXPSON2+	Channel 2 PS enable source
34	COM	Channel 2 PS common
35	TXPSD2+	Channel 2 PS data source
36	COM	Channel 2 PS common

9.6. SPECIFICATIONS/ASSEMBLY DIFFERENCES

Table 9–4. NVTWC-MOD Board Specifications

Specification	31166-099	
	-01	-02
Maximum Number of Boards Per CSEX Subsystem	8	
Board Slots Required	1	
Maximum Board Logic Current Supply Draw	350 mA	
Number of Channels	4	
Maximum Baud Rate	50	
Maximum Detection Frequency	10 kHz	
Software	Basic board without software	2 Channel TWC Transmit/Receive (40026-237)

10. SECTION 10 – NVTWC-MUX (NON-VITAL TWC MULTIPLEXER) BOARD, P/N 31166-100-XX

10.1. GENERAL

The purpose of the Non-Vital Train-To-Wayside Communications Multiplexer (NVTWC-MUX) board is to process bit streams of TWC information as received from other field equipment. These bit streams are then reformatted so that they can then be sent to the CSEX3 Board. The digital portion of this board is very similar to the Non-Vital TWC Modem Board. However, instead of the four analog bandpass filters, this board contains 24 Non-Vital optically isolated inputs and 8 Non-Vital optically isolated outputs. In this manner, the NVTWC-MUX board can be thought of as a “smart” Non-Vital I/O interface. This board can be configured (by Alstom) to meet a variety of applications. An on-board microprocessor and FPGAs (programmable hardware) allow a considerable degree of flexibility.

See Figure A–10 for a board layout drawing.

10.2. OPERATION

Menu driven board diagnostics can be accessed with a VT100 terminal or equivalent. The diagnostics allows the user to view incoming receive messages, transmit messages and to view commands to and from the CSEX3 Board. Additional information for a specific application can be found in Alstom specific system manuals.

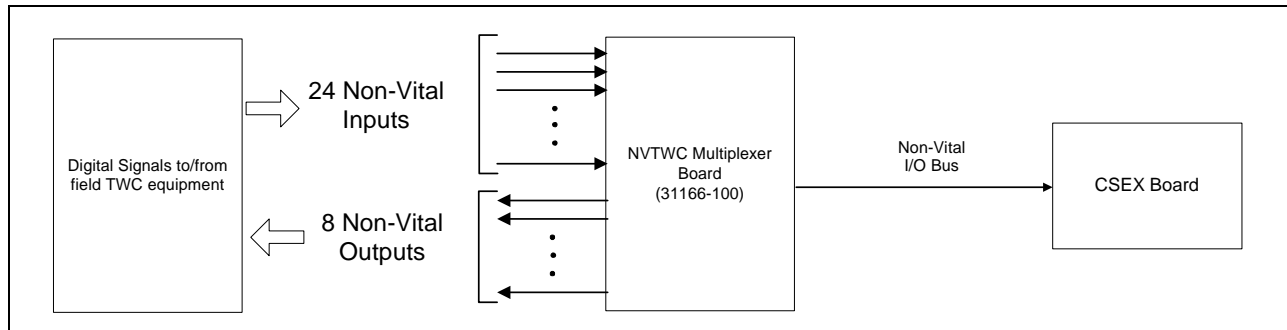


Figure 10–1. NVTWC-MUX Board Subsystem Block Diagram

10.3. INDICATIONS

Figure 10–2 shows the NVTWC-MUX board LED indications.
























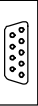


NORMAL INDICATION	PCB NOTATION	FUNCTION
	S1	 RESET (Reset Switch)
ON, OFF	DS1	 (Channel #4 TX Data)
ON, OFF	DS2	 (Channel #4 RX Data)
ON, OFF	DS3	 (Channel #4 PS Data)
ON, OFF	DS4	 (Channel #4 18Hz Bit Clock)
ON, OFF	DS5	 (Channel #4 3Hz Track Sync)
ON, OFF	DS6	 (Channel #3 TX Data)
ON, OFF	DS7	 (Channel #3 RX Data)
ON, OFF	DS8	 (Channel #3 PS Data)
ON, OFF	DS9	 (Channel #3 18Hz Bit Clock)
ON, OFF	DS10	 (Channel #3 3Hz Track Sync)
ON, OFF	DS11	 (Board Select)
ON, OFF	DS12	 (Channel #2 TX Data)
ON, OFF	DS13	 (Channel #2 RX Data)
ON, OFF	DS14	 (Channel #2 PS Data)
ON, OFF	DS15	 (Channel #2 18Hz Bit Clock)
ON, OFF	DS16	 (Channel #2 3Hz Track Sync)
ON, OFF	DS17	 (Channel #1 TX Data)
ON, OFF	DS18	 (Channel #1 RX Data)
ON, OFF	DS19	 (Channel #1 PS Data)
ON, OFF	DS20	 (Channel #1 18Hz Bit Clock)
ON, OFF	DS21	 (Channel #1 3Hz Track Sync)
OFF	DS22	 (Reset)
	J2	 (MAC Port)
	E1	 COM (Common Test Point)
	E2	 +5V (+5 Volts Test Point)

Figure 10–2. NVTWC-MUX Board Edge

10.4. TEST POINTS

Figure 10–3 shows the NVTWC-MUX port, switch and test point locations.

Table 10–1. NVTWC-MUX Board Test Points

Test Point	Function
E1	+5V logic power
E2	COM, logic common

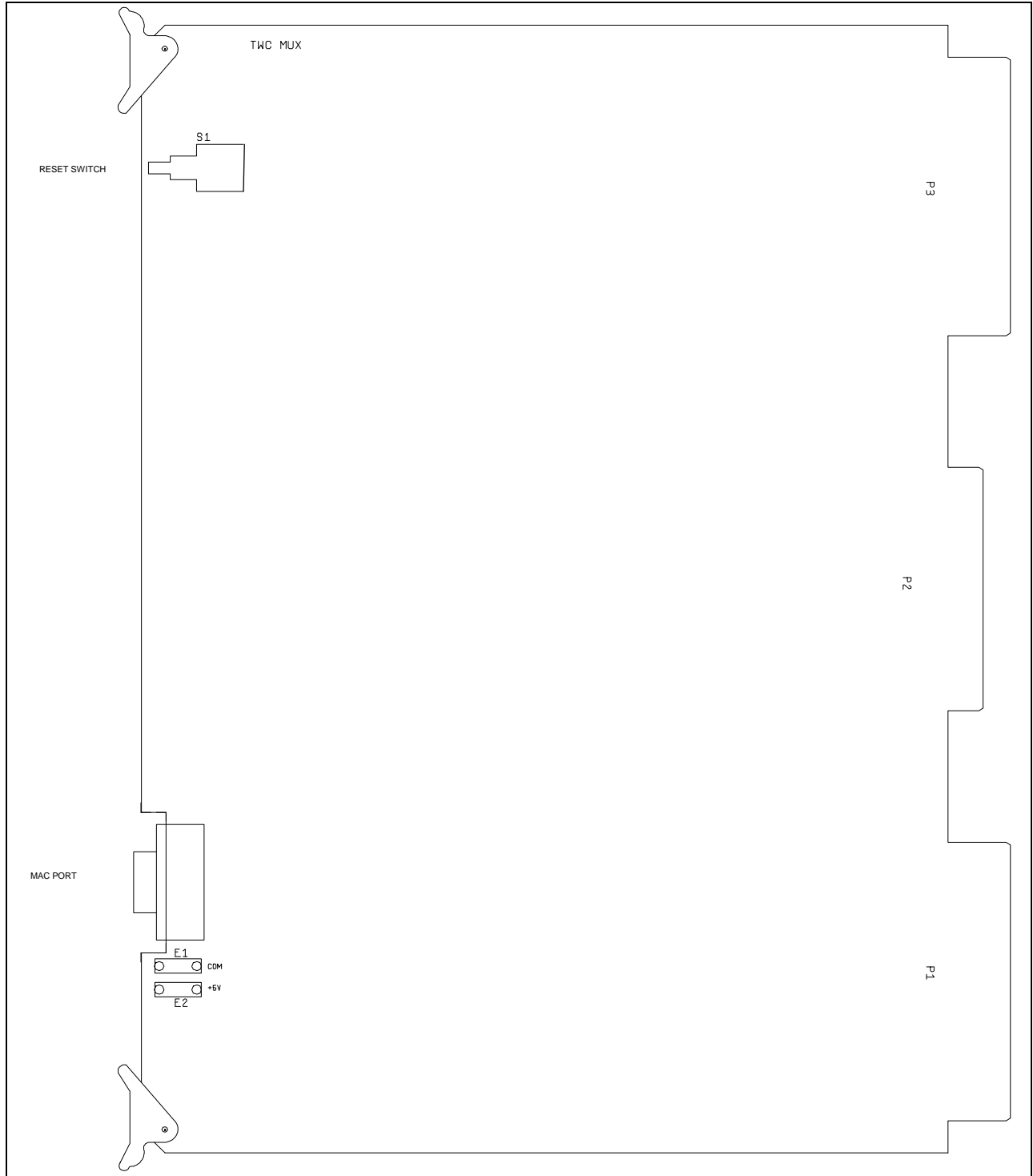


Figure 10–3. NVTWC-MUX Board Port, Switch, Test Point Locations

10.5. CARD EDGE CONNECTORS

The NVTWC-MUX Board has three card edge connectors.

- P3, the top connector, is a 36-pin connector which contains wiring for Channels 3 and 4 and power supply connections
 - See Table 10–2 for 36-pin configuration details
- P2, the middle connector, is a 50-pin connector used for communication with a CSEX board, and also to supply +5V logic power
 - P2-42 through P2-47 are wired in a specific pattern to common P2-48 per the application .lvc CAAPE report for board addressing; the remaining P2 pins are not user configurable
- P1, the lower connector, is a 36-pin connector which contains wiring for Channels 1 and 2 and power supply connections
 - See Table 10–3 for 36-pin configuration details

NOTE

For the user defined inputs and outputs, refer to the .lvc output file generated by the CAAPE program.

Table 10–2. NVTWC-MUX Board 36-pin P3 Connections

P3-	Name	Function
1	RXID3+	Channel 3 receive data drive
2	RXID3-	Channel 3 receive data return
3	18HZIN3+	Channel 3 18Hz clock drive
4	18HZIN3-	Channel 3 18Hz clock return
5	PHSAIN3+	Channel 3 Phase A sync drive
6	PHSAIN3-	Channel 3 Phase A sync return
7	PHSBIN3+	Channel 3 Phase B sync drive
8	PHSBIN3-	Channel 3 Phase B sync return
9	SRCSEL3+	Channel 3 default transmit
10	COM	+5V common
11	SPARIN2+	(not used)
12	SPARIN2-	(not used)
13	TXID_3	Channel 3 transmit data
14	TXPS_3	Channel 3 program stop data
15	WPIN3_4+	Data-Back channel 2 word-pulse drive
16	WPIN3_4-	Data-Back channel 2 word-pulse return
17	VDC_CH3+	Channel 3 transmit/program stop drive
18	VDC_CH3-	Channel 3 transmit/program stop return
19	DBIN3_4+	Data-Back channel 2 data drive
20	DBIN3_4-	Data-Back channel 2 data return
21	576HZ34+	Data-Back channel 2 576Hz clock drive
22	576HZ34-	Data-Back channel 2 576Hz clock return
23	RXID4+	Channel 4 receive data drive
24	RXID4-	Channel 4 receive data return
25	18HZIN4+	Channel 4 18Hz clock drive
26	18HZIN4-	Channel 4 18Hz clock return
27	PHSAIN4+	Channel 4 Phase A sync drive
28	PHSAIN4-	Channel 4 Phase A sync return
29	PHSBIN4+	Channel 4 Phase B sync drive
30	PHSBIN4-	Channel 4 Phase B sync return

Table 10–2. NVTWC-MUX Board 36-pin P3 Connections (Cont.)

P3-	Name	Function
31	SRCSEL4+	Channel 4 default transmit
32	COM	+5V common
33	TXID_4	Channel 4 transmit data
34	TXPS_4	Channel 4 program stop data
35	VDC_CH4+	Channel 4 transmit/program stop drive
36	VDC_CH4-	Channel 4 transmit/program stop return

Table 10–3. NVTWC-MUX Board 36-pin P1 Connections

P1-	Name	Function
1	RXID1+	Channel 1 receive data drive
2	RXID1-	Channel 1 receive data return
3	18HZIN1+	Channel 1 18Hz clock drive
4	18HZIN1-	Channel 1 18Hz clock return
5	PHSAIN1+	Channel 1 Phase A sync drive
6	PHSAIN1-	Channel 1 Phase A sync return
7	PHSBIN1+	Channel 1 Phase B sync drive
8	PHSBIN1-	Channel 1 Phase B sync return
9	SRCSEL1+	Channel 1 default transmit
10	COM	+5V common
11	SPARIN1+	(not used)
12	SPARIN1-	(not used)
13	TXID_1	Channel 1 transmit data
14	TXPS_1	Channel 1 program stop data
15	WPIN1_2+	Data-Back channel 1 word-pulse drive
16	WPIN1_2-	Data-Back channel 1 word-pulse return
17	VDC_CH1+	Channel 1 transmit/program stop drive
18	VDC_CH1-	Channel 1 transmit/program stop return
19	DBIN1_2+	Data-Back channel 1 data drive
20	DBIN1_2-	Data-Back channel 1 data return
21	576HZ12+	Data-Back channel 1 576Hz clock drive
22	576HZ12-	Data-Back channel 1 576Hz clock return
23	RXID2+	Channel 2 receive data drive
24	RXID2-	Channel 2 receive data return
25	18HZIN2+	Channel 2 18Hz clock drive
26	18HZIN2-	Channel 2 18Hz clock return
27	PHSAIN2+	Channel 2 Phase A sync drive
28	PHSAIN2-	Channel 2 Phase A sync return
29	PHSBIN2+	Channel 2 Phase B sync drive
30	PHSBIN2-	Channel 2 Phase B sync return

Table 10–3. NVTWC-MUX Board 36-pin P1 Connections (Cont.)

P1-	Name	Function
31	SRCSEL2+	Channel 2 default transmit
32	COM	+5V common
33	TXID_2	Channel 2 transmit data
34	TXPS_2	Channel 2 program stop data
35	VDC_CH2+	Channel 2 transmit/program stop drive
36	VDC_CH2-	Channel 2 transmit/program stop return

10.6. SPECIFICATIONS

Table 10–4. NVTWC-MUX Board Specifications

Specification	31166-100-02
Maximum Number of Boards Per CSEX Subsystem	8
Board Slots Required	1
Maximum Board Logic Current Supply Draw	350 mA
External Power Supply Requirements	6-12 VDC, 8A
Number of Inputs	24
Voltage Range of Inputs	6-20 VDC
Frequency Range of inputs	0 - 1000 Hz
Number of Outputs	8
Maximum Output Current Per Port	1A (source/sink)
Maximum Output Steady State Power Per Port	5 Watts
Frequency Range of Outputs	0 - 1000 Hz

A. APPENDIX A – NON-VITAL BOARD LAYOUT DRAWINGS

A.1. GENERAL

This appendix contains layout drawings of the boards discussed in this manual.

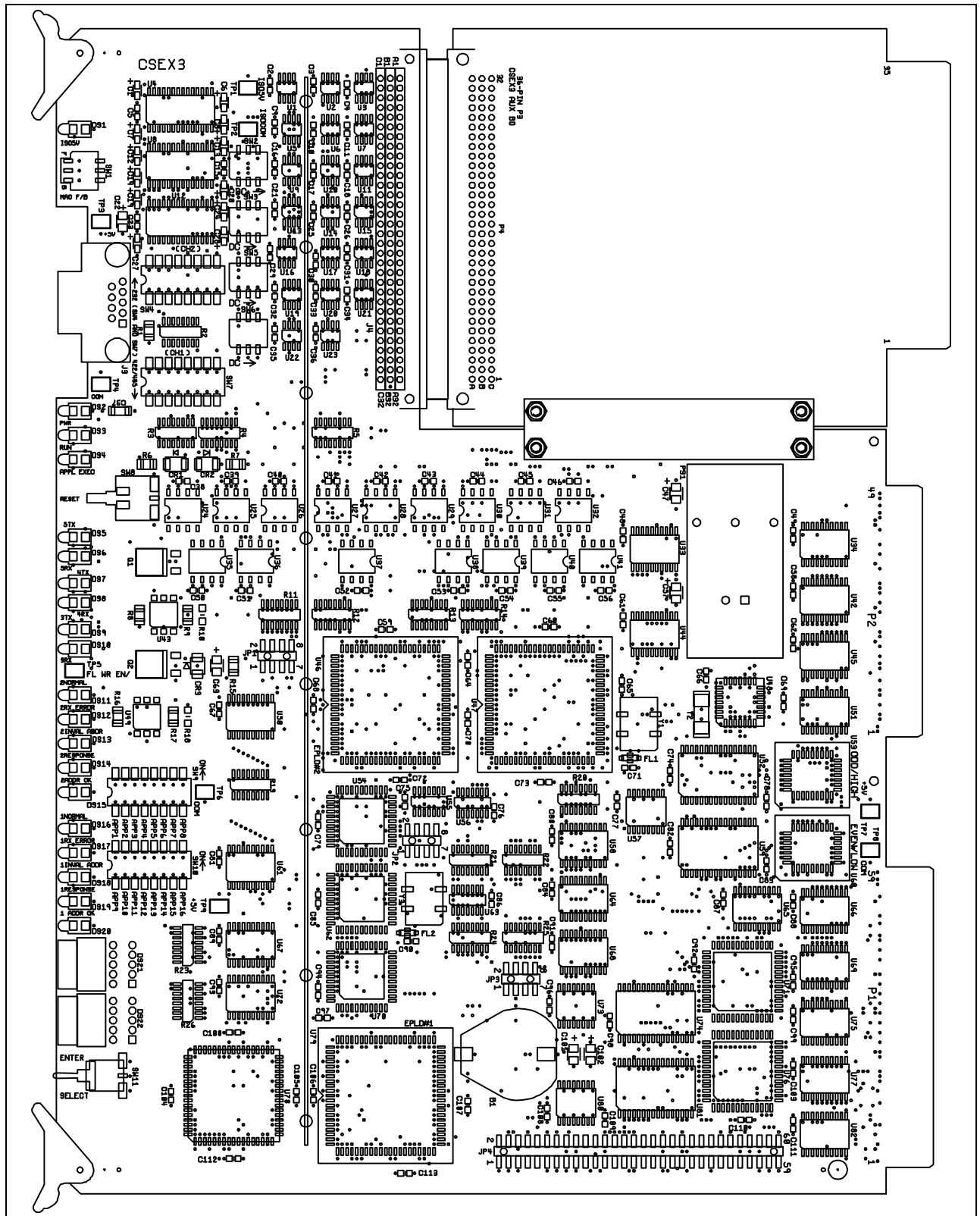


Figure A-1. CSEX3 Board, P/N 31166-175-00

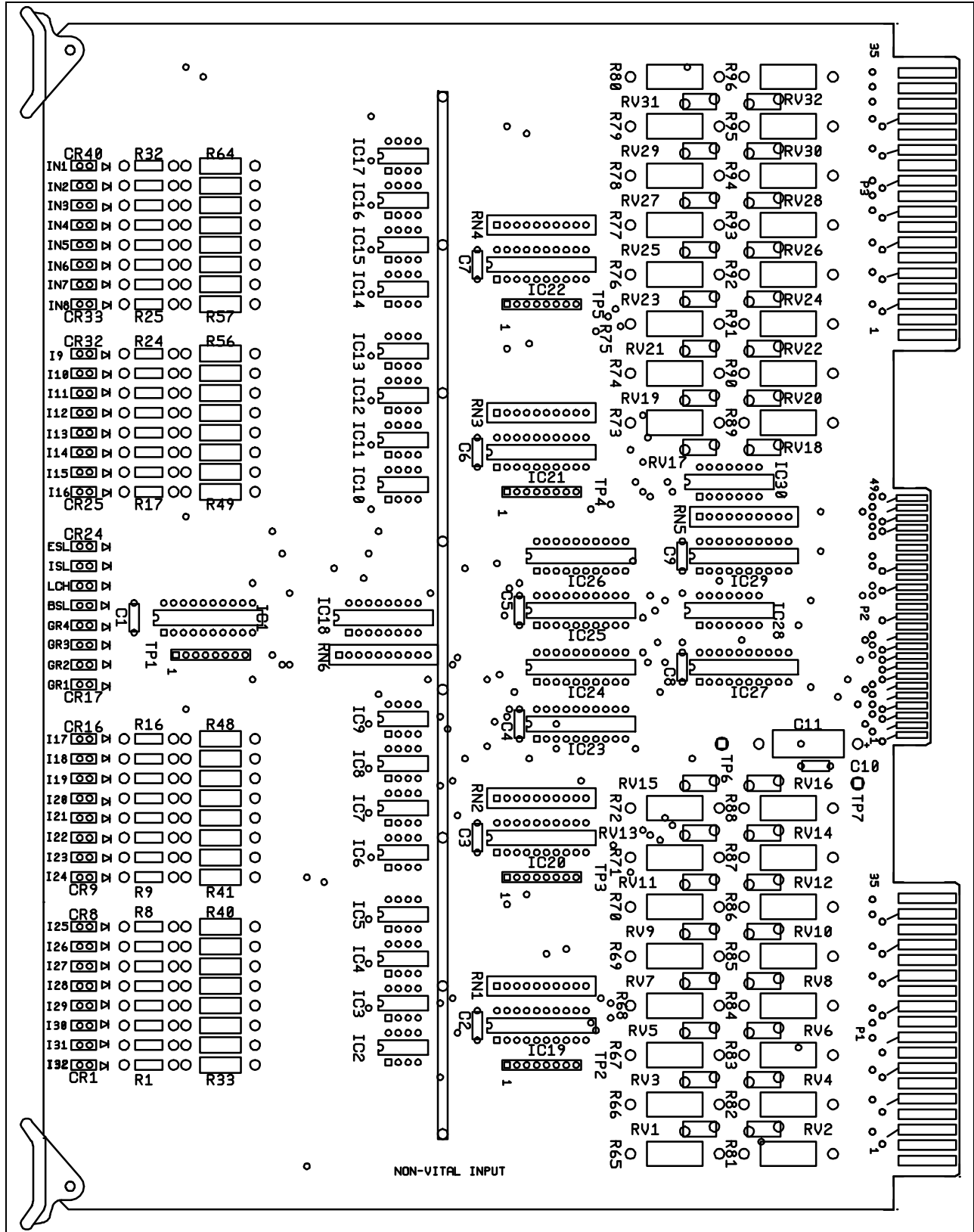


Figure A-2. NVI Board, P/N 59473-757-00

Non-Vital Board Layout Drawings

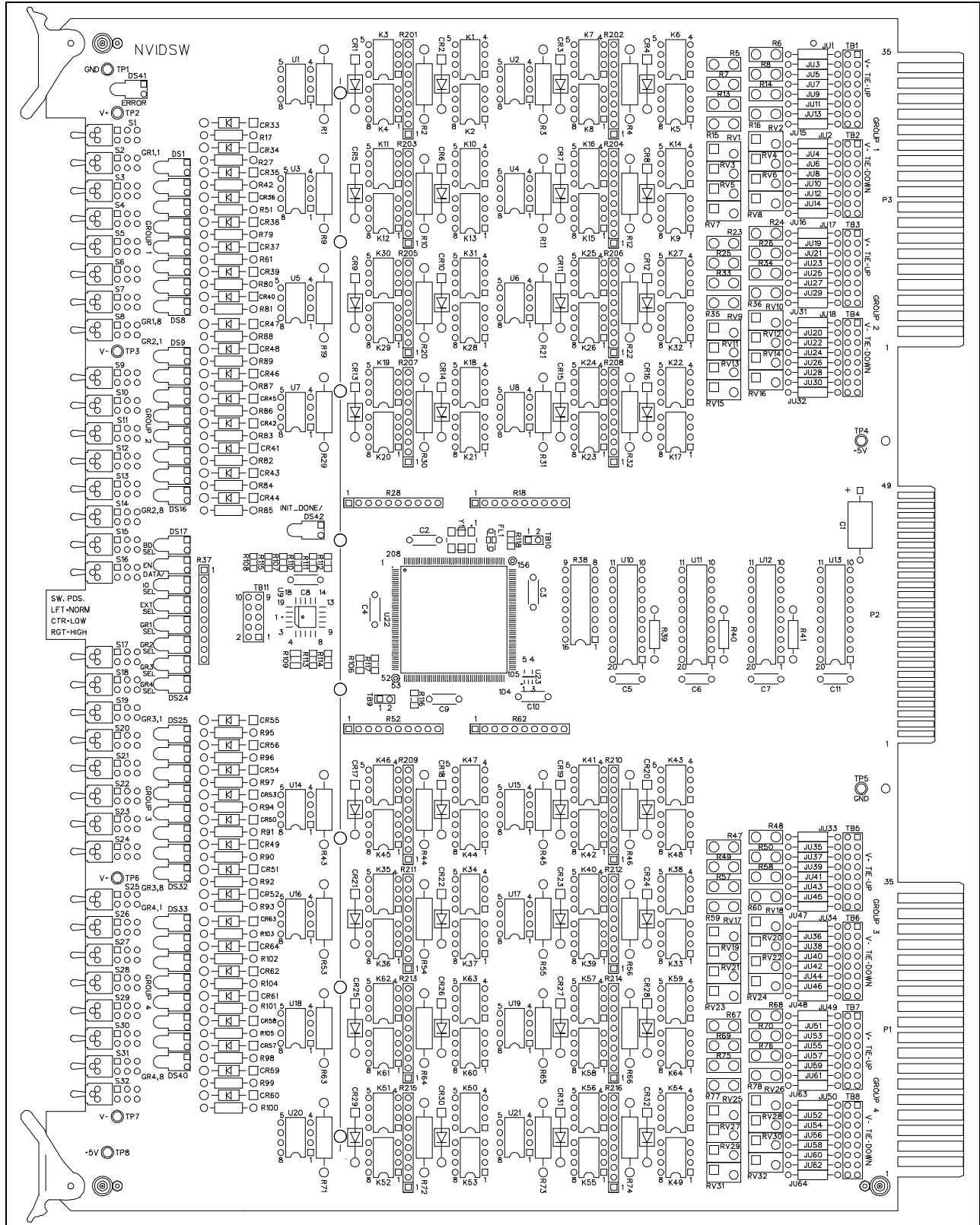


Figure A-3. NVIDSW Board, P/N 31166-276-00

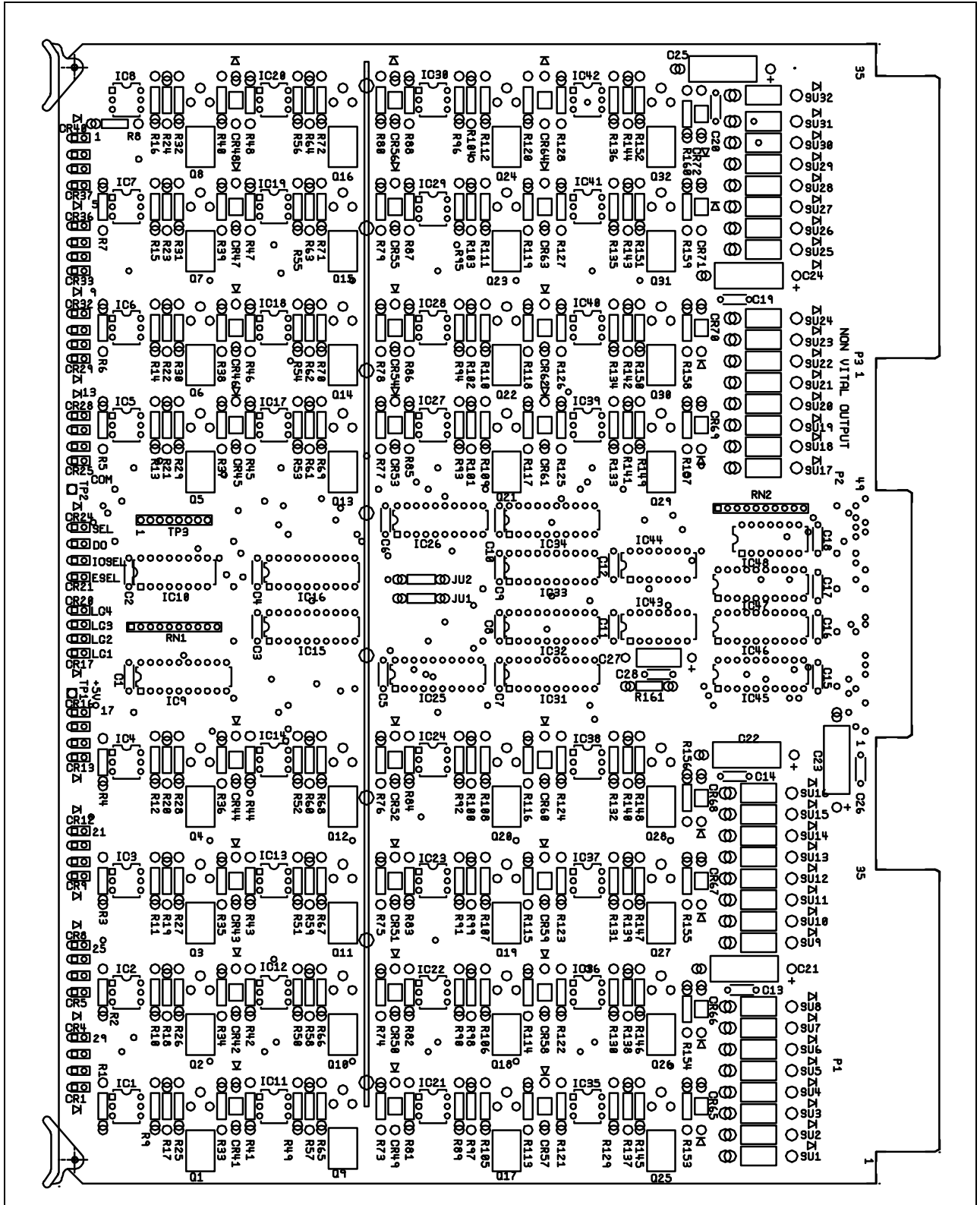


Figure A-4. NVO Board, P/N 59473-785-00

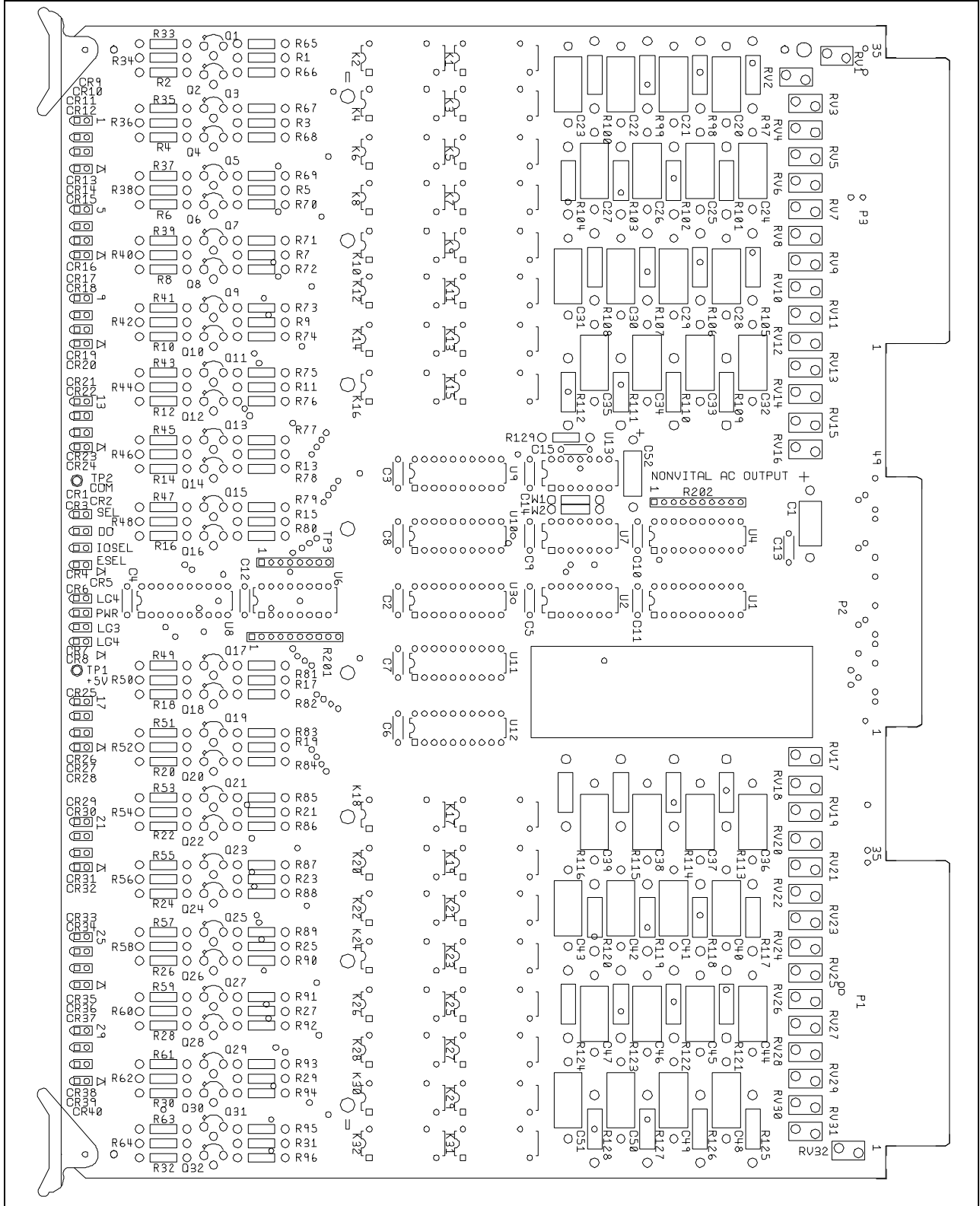


Figure A-5. NVOAC Board, P/N 59473-936-00

Non-Vital Board Layout Drawings

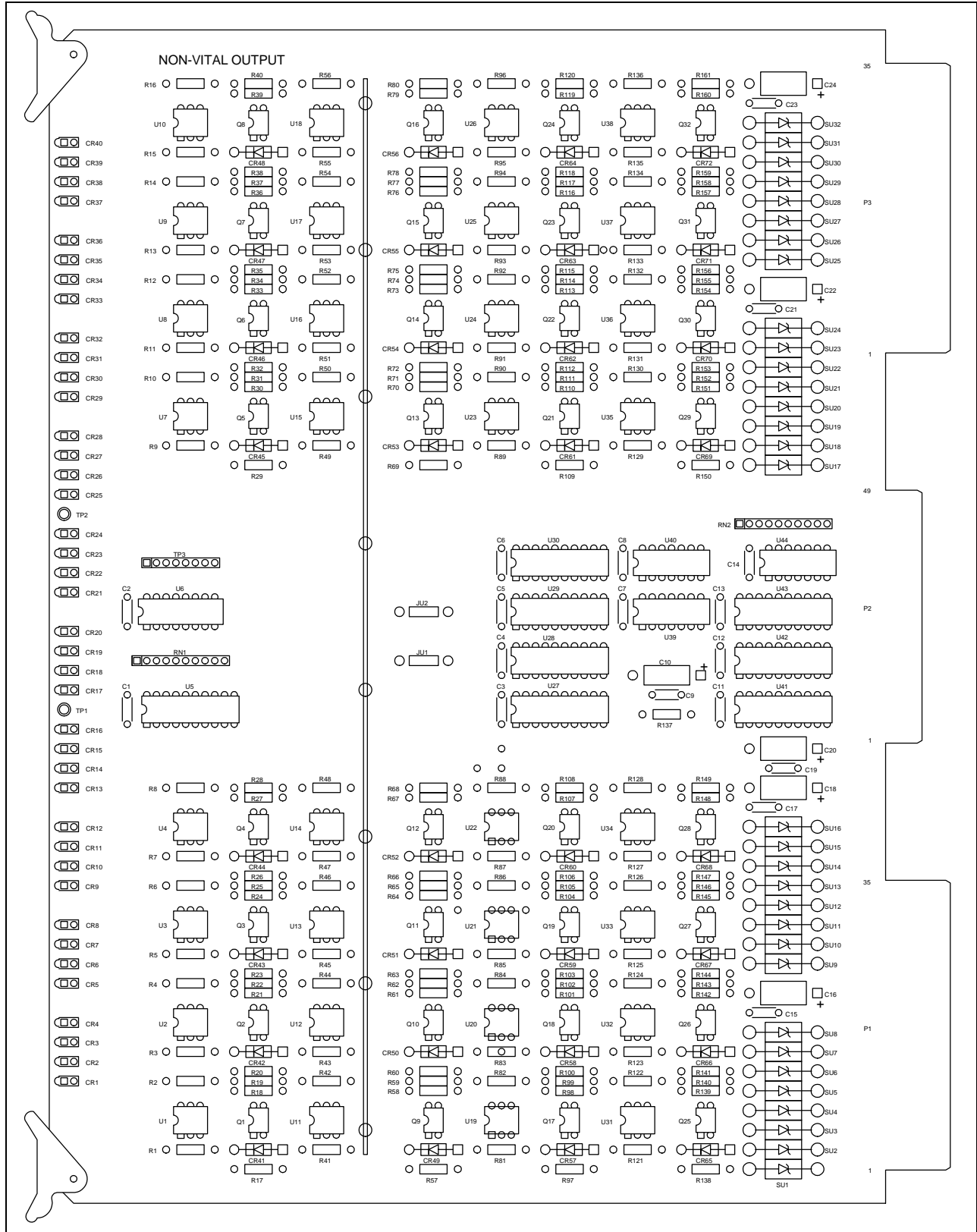


Figure A-6. NVO-SNK Board, P/N 31166-123-00

Non-Vital Board Layout Drawings

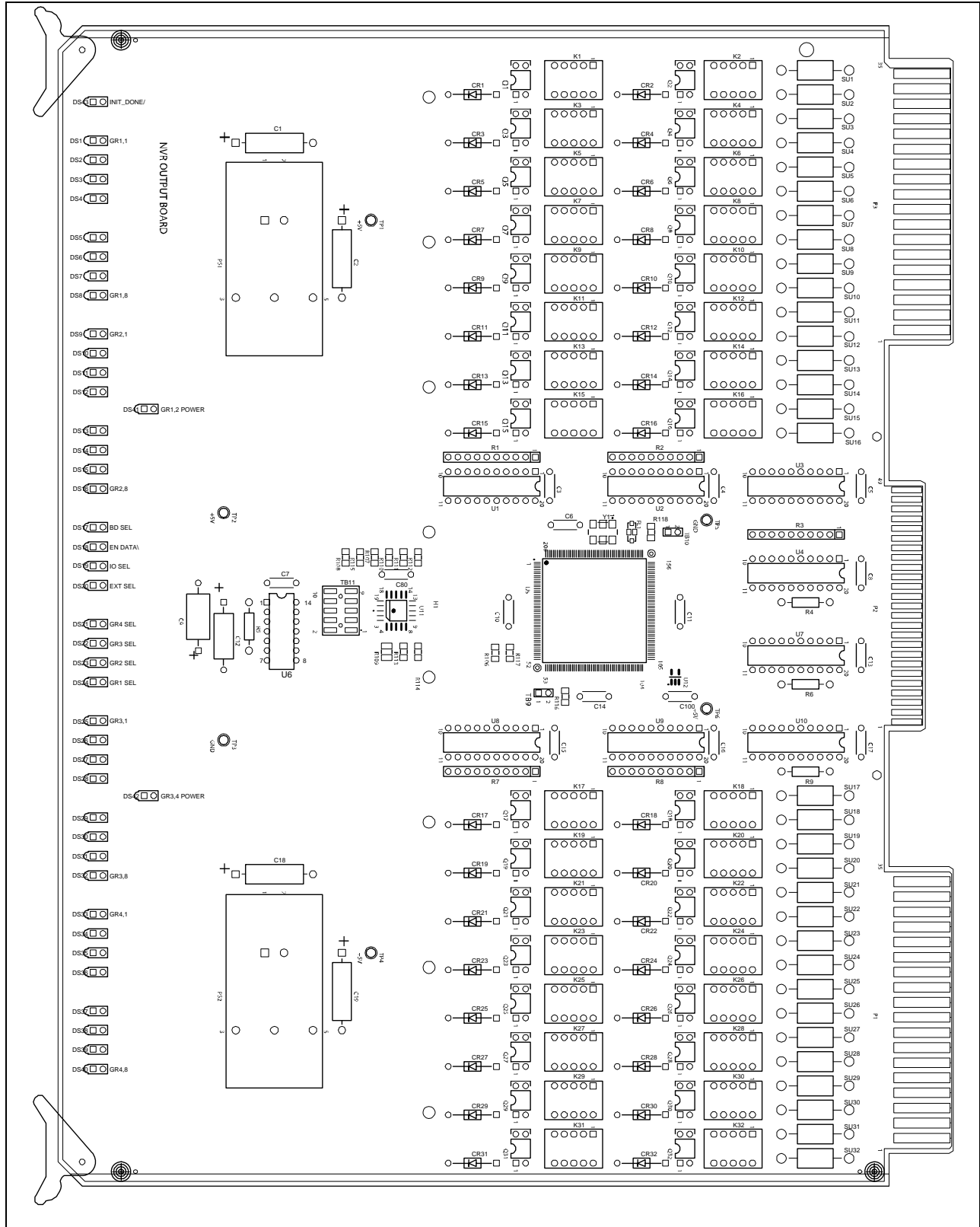


Figure A-7. NVR Board, P/N 31166-238-00

Non-Vital Board Layout Drawings

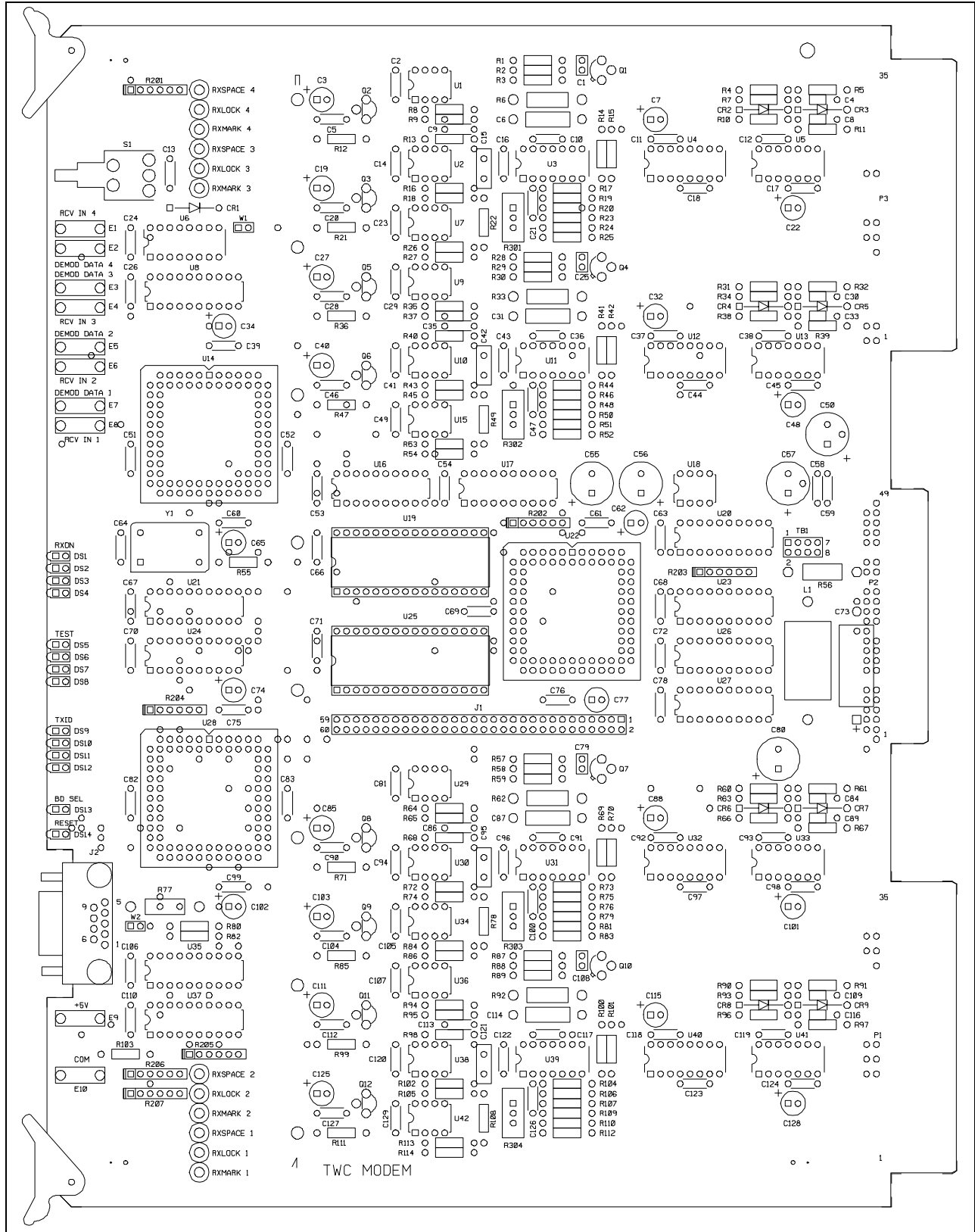


Figure A-8. NVTWC-FSK Board, P/N 31166-119-00

Non-Vital Board Layout Drawings

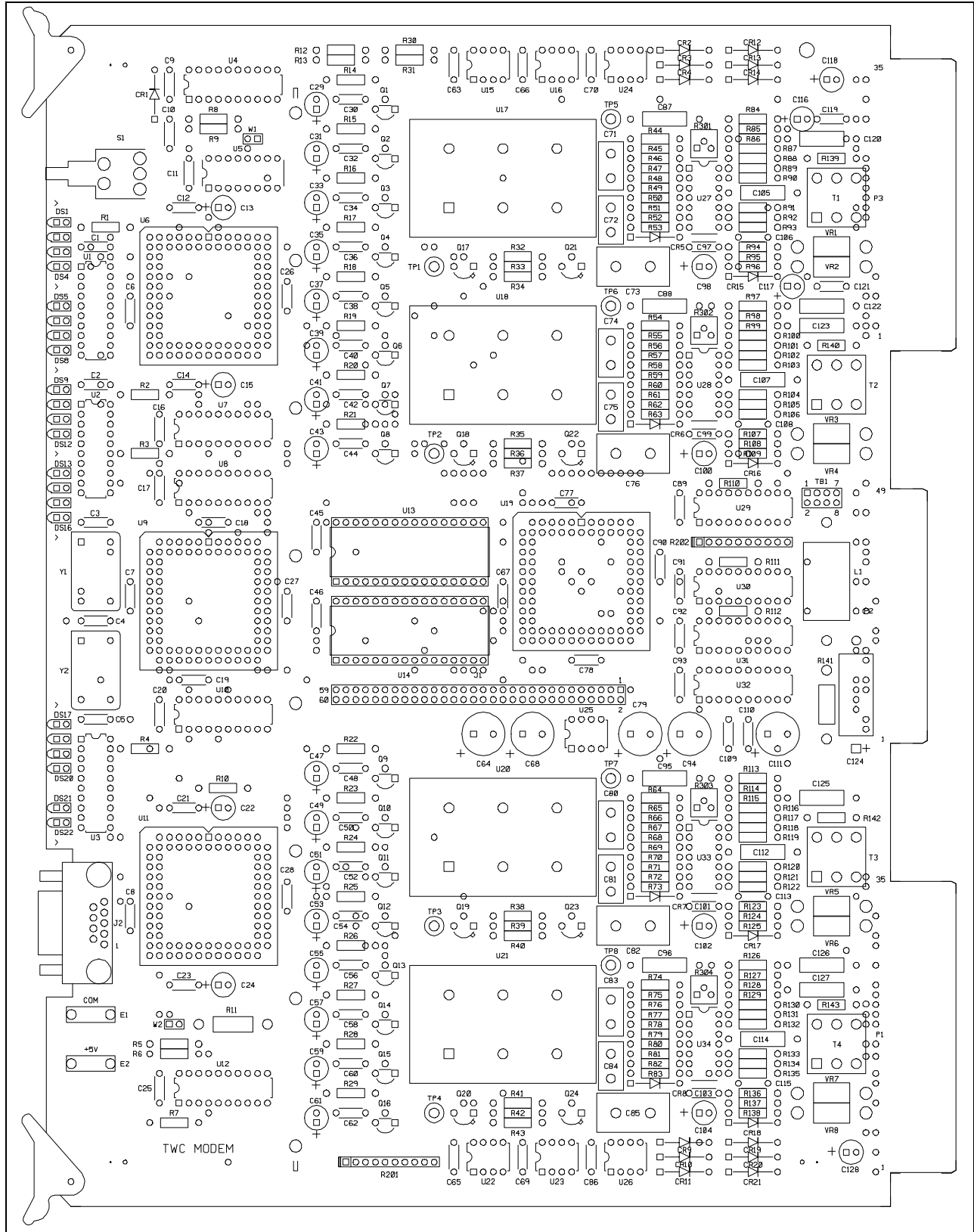


Figure A-9. NVTWC-MOD Board, P/N 31166-099-00

Non-Vital Board Layout Drawings

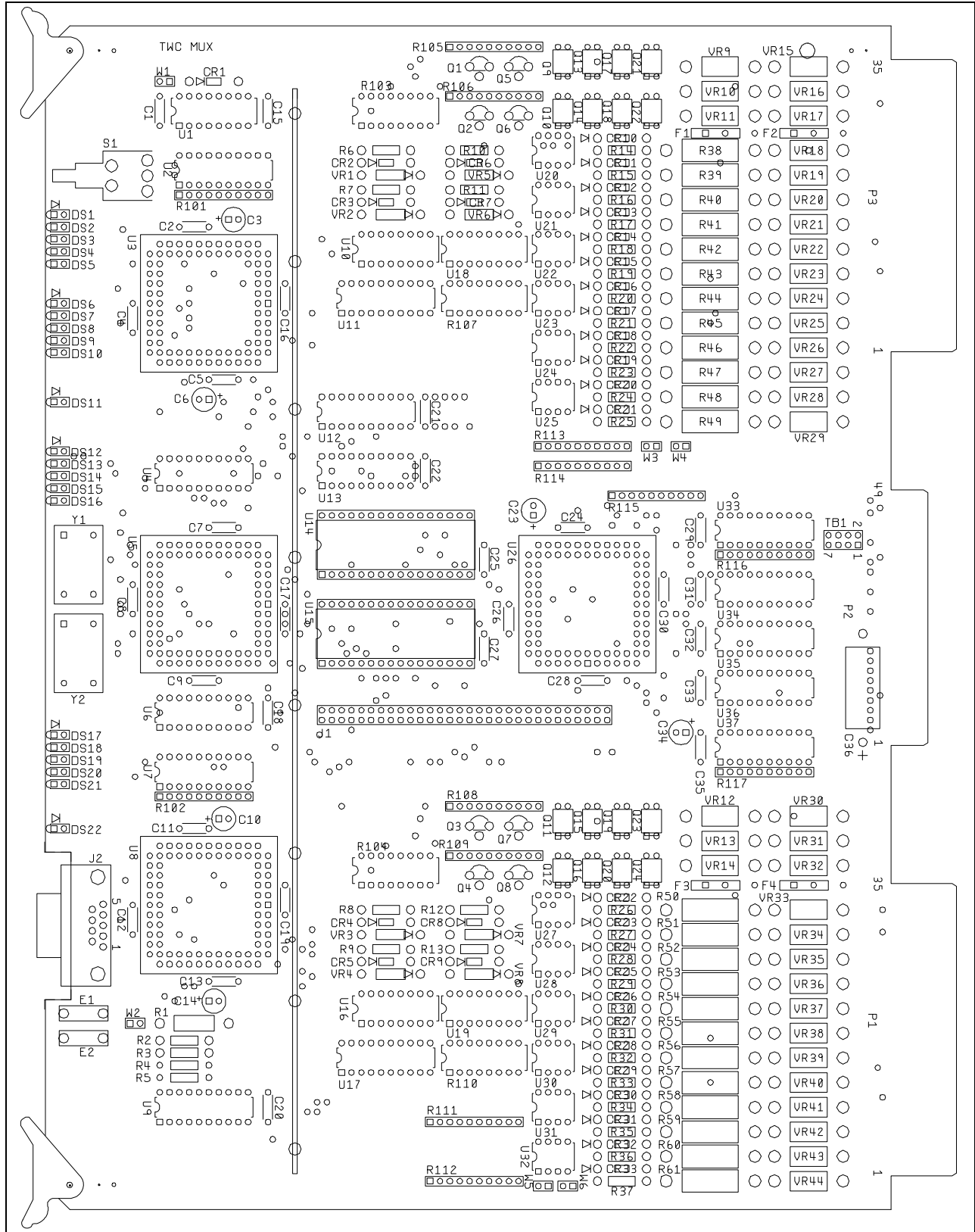


Figure A-10. NVTWC-MUX Board, P/N 31166-100-00

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