ALSTOM

VPI® II

Vital Processor Interlocking Control System

Vital Subsystem

Vital Subsystem Manual
P2511B, Volume 3

ALSTOM

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Vital Processor Interlocking Control System

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Vital Subsystem Manual
Alstom Signaling Inc.

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PREFACE

NOTICE OF CONFIDENTIAL INFORMATION

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REVISION LOG

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0	August 2008	Original issue.	MAS	KW	NI
1	May 2011	Added CPU II Comm Panel, updated DBO, LDO, and LDO2 Boards.	MAS	RIH	NI

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ABOUT THE MANUAL

This manual is intended to describe the Alstom Vital Processor Interlocking Control System, (VPI® II) Vital subsystem (Vital boards). This manual is part of a 5 volume set of manuals. The set is summarized in Section 1.

The information in this manual is arranged into sections. The title and a brief description of each section follow:

Section 1 – VITAL PRINTED CIRCUIT BOARDS: This section summarizes the VPI® II Vital subsystem boards.

Section 2 – CPU II (CENTRAL PROCESSING UNIT II) BOARD, P/N 31166-374-XX: This section provides CPU II board detail, including discussion of the CPU2 Interface Board (P/N 31166-499-XX).

Section 3 – VRD (VITAL RELAY DRIVER) BOARD, P/N 59473-740-02: This section provides VRD board detail.

Section 4 – VSC (VITAL SERIAL CONTROLLER) BOARD, P/N 59473-939-XX: This section provides VSC board detail.

Section 5 – CRG (CODE RATE GENERATOR) BOARD, P/N 31166-261-XX: This section provides CRG board detail.

Section 6 – IOB (I/O BUS INTERFACE) BOARD, P/N 59473-827-XX: This section provides IOB board detail.

Section 7 – DI (DIRECT INPUT) BOARD, P/N 59473-867-XX: This section provides DI board detail.

Section 8 – VITAL DC OUTPUT BOARDS, P/N 59473-739-XX, -747-XX, -977-XX, -749-XX, 31166-340-XX: This section provides Vital DC output board detail.

Section 9 – ACO (AC OUTPUT) BOARD, P/N 59473-937-XX: This section provides Vital ACO board detail.

Section 10 – FSVT (FIELD-SETTABLE VITAL TIMER) BOARD, P/N 59473-894-XX: This section provides FSVT board detail.

Appendix A – SIGNATURE HEADERS AND PROMS: This appendix provides VPI circuit boards Signature Header and PROM information.

Appendix B – VITAL BOARD LAYOUT DRAWINGS: This appendix provides the layout drawings for each Vital board type.

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MANUAL SPECIAL NOTATIONS

In the Alstom manuals, there are three methods used to convey special informational notations to the reader. These notations are warnings, cautions, and notes. Both warnings and cautions are readily noticeable by boldface type two lines beneath the caption.

Warning

A warning is the most important notation to heed. A warning is used to tell the reader that special attention needs to be paid to the message because if the instructions or advice is not followed when working on the equipment then the result could be either serious harm or death. The sudden, unexpected operation of a switch machine, for example, or the technician contacting the third rail could lead to personal injury or death. An example of a typical warning notice follows:

WARNING

DISCONNECT MOTOR ENERGY WHENEVER WORKING ON SWITCH LAYOUT OR SWITCH MACHINE. UNEXPECTED OPERATION OF MACHINE COULD CAUSE INJURY FROM OPEN GEARS, ELECTRICAL SHOCK, OR MOVING SWITCH POINTS.

Caution

A caution statement is used when an operating or maintenance procedure, practice, condition, or statement, which if not strictly adhered to, could result in damage to or destruction of equipment. A typical caution found in a manual is as follows:

CAUTION

Turn power off before attempting to remove or insert circuit boards into a module. Boards can be damaged if power is not turned off.

Note

A note is normally used to provide minor additional information to the reader to explain the reason for a given step in a test procedure or to just provide a background detail. An example of the use of a note follows:

NOTE

A capacitor may be mounted on the circuit board with a RTV adhesive. Use the same color RTV.

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1. SECTION 1 – VITAL PRINTED CIRCUIT BOARDS

1.1. INTRODUCTION

This manual describes the Printed Circuit Boards used to provide Vital functionality in the VPI II System. It includes a brief description of the differences between board variations and the keying information for all variations of each board type.

1.2. GENERAL

This section summarizes the VPI® II Vital subsystem boards.

1.3. MANUAL SET ORGANIZATION

This manual is part of a 5 volume set supporting the VPI II system. The set is organized as follows:

- Volume 1, Installation, Operation, and Theory Manual, includes general overview of the field installation and setup of the VPI II system; including capacity guidelines and allowable VSC/CSEX board combinations, system operation, and theory of operation.
- Volume 2, Chassis Configuration, describes the chassis configuration including cables and power supplies.
- Volume 3, Vital Subsystem, is this document. It includes the Vital subsystem board drawings, signature headers and proms, and board reference data.
- Volume 4, Non-Vital Subsystem, includes non-vital subsystem board drawings and board reference data.
- Volume 5, Maintenance and Troubleshooting, describes system maintenance and troubleshooting, including discussion of diagnostics and references for the applicable software and hardware manuals.

1.3.1. Vital Subsystem

Figure 1–1 is a block diagram of the boards in the Vital and non-vital subsystems.

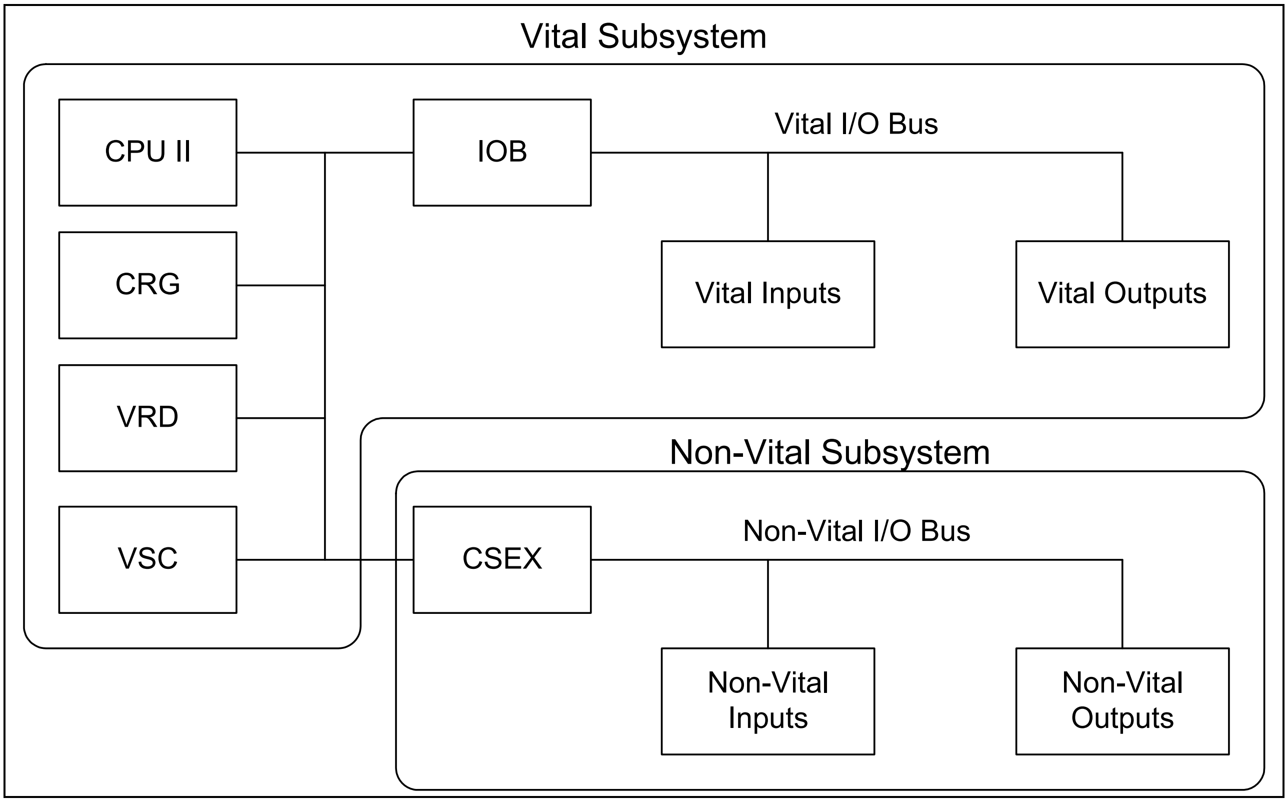

Figure 1–1. Vital and Non-Vital Subsystems

Table 1–1 lists the Vital printed circuit boards in the order that they are discussed. A board's 10 digit drawing number is also the part number to use for ordering the board.

Table 1–1. Vital PC Boards Index

Board Type	Drawing Number	Comments
CPU II	31166-374-01	Vital Processor
CPU II	31166-374-02	Vital Processor with Ethernet Network Communications
VRD	59473-740-02	Vital Relay Driver
VSC	59473-939-10	Pt.-Pt. w/40025-322-00 VSC software
VSC	59473-939-11	Pt.-Pt. w/ EIA232 Daughterboard w/40025-322-00 VSC software

Table 1–1. Vital PC Boards Index (Cont.)

Board Type	Drawing Number	Comments
VSC	59473-939-12	Multidrop w/40025-323-00 MVSC software
VSC	59473-939-13	Multidrop, half duplex w/40025-324-00 GVSC software
VSC	59473-939-14	Multidrop, half duplex w/40025-348-00 GVSCE software
VSC	59473-939-17	Pt.-Pt. w/40025-406-00 VSC software
VSC	59473-939-18	Pt.-Pt. w/ EIA232 Daughterboard w/40025-406-00 VSC software
CRG	31166-261-03	Solid State Relay Driver w/40025-235-00 software, supports code rates 0, 50, 75, 120, 180 pulses per minute (PPM)
CRG	31166-261-04	B-Relay Driver w/40025-325-00 software, supports code rates 0, 50, 75, 120, 180, 270, 420 pulses per minute (PPM), and steady ON
IOB	59473-827-01	Vital I/O Bus Interface Board
DI	59473-867-01	(16) 9-15 VDC, low-pass filter
DI	59473-867-02	(16) 9-15 VDC, no low-pass filter
DI	59473-867-03	(16) 9-15 VDC, momentary input hold
DI	59473-867-04	(16) 45-55 VDC, low-pass filter
DI	59473-867-05	(16) 9-22 VDC, low-pass filter
DI	59473-867-07	(16) 24-34 VDC, low-pass filter
SBO	59473-739-01	(8) 9-30 VDC, 0.5 A
SBO	59473-739-02	(8) 9-30 VDC, 0.5 A, , does not provide any filtering of the external output supply voltage
DBO	59473-747-01	(8) 9-15 VDC, 0.6 A, Vout=Vin – 5*Iout, (nominal 12 VDC source/12 VDC out)
DBO	59473-747-02	(8) 9-15 VDC, 0.3 A, Vout=2.3*Vin – 10 *Iout (nominal 12 VDC source/24 VDC out)
DBO	59473-747-03	59473-747-01 with different keying than -747-01
DBO-50V	59473-977-01	(8) 50 VDC @ 0.14 A out, 30-40 VDC in
DBO-50V	59473-977-02	(8) 50 VDC @ 0.14 A out, 45-55 VDC in
LDO	59473-749-02	(8) 9-18 VDC, 2.9 A, 100 mA Hot/Cold check
LDO	59473-749-03	(8) 15-30 VDC, 2.9 A, 200 mA Hot/Cold check
LDO	59473-749-04	(8) 9-18 VDC, 2.9 A, 100 mA without Cold check

Table 1–1. Vital PC Boards Index (Cont.)

Board Type	Drawing Number	Comments
LDO2	31166-340-01	(8) 9-18VDC, 3.3A
LDO2	31166-340-02	(8) 9-18VDC, 3.3A (without current monitor)
ACO	59473-937-01	(8) 90-130 VAC, 0.8 A, 40-150 HZ (superseded by -02)
ACO	59473-937-02	(8) 90-130 VAC, 0.8 A, 40-150 HZ (higher EMI protection)
ACO	59473-937-03	(8) 90-130 VAC, 0.5 A, 40-150 HZ (higher EMI protection)
FSVT	59473-894-01	(8) Field-Settable Vital Timers # 1-8
FSVT	59473-894-02	(8) Field-Settable Vital Timers # 9-16

Each board contains three card edge connectors, identified as P3, P2 and P1 from top to bottom. These connections are described for each system board in the sections that follow.

Refer to the .lvc output file generated by the system software CAAPE program for wire wrap specifications and the user defined inputs and outputs. For additional information on this program, refer to the following Alstom manuals:

- P2412A, CAAPE Users Guide
- P2412B, CAAPE AlsDload
- P2412D, VPI CAA Reference

NOTE

A VPI II System performing non-vital functions can be configured with either a Code System Emulator Extended 3 or 4 (CSEX3 or CSEX4) non vital processor board. This manual uses the generic term CSEX unless a function is specific to CSEX3 or CSEX4. See P2511B, Volume 4 for discussions of the two boards.

2. SECTION 2 – CPU II (CENTRAL PROCESSING UNIT II) BOARD, P/N 31166-374-XX

2.1. INTRODUCTION

This section provides CPU II board detail, including discussion of the CPU2 Interface Board (P/N 31166-499-XX).

2.2. GENERAL

The CPU II board is designed as a system board for VPI II incorporating Vital logic processing, Vital I/O control and monitoring, and an extended capacity for larger interlockings. The board includes vital communications, logic voltage monitoring, USB, on-board programming, and Ethernet connectivity. The board contains primarily SMT (Surface Mount Technology) parts.

The CPU II contains two 32-bit 80386EX33 microprocessors that separately perform the Vital processing and high-speed communications functions.

See P2511B, Volume 1, Table 2–3 for board limits / application criteria.

Figure 2–1. CPU II Board

2.3. ASSEMBLY

Table 2–1. CPU II Board Assembly

Description	Part Number
Vital Processor	31166-374-01
31166-374-01 with a Communications Processor for Ethernet Network Communications	31166-374-02

2.4. FUNCTION

All control and monitoring functions for the VPI module go through the CPU II board.

Once each second:

- inputs are read
- all expressions are evaluated
- outputs are updated

In addition, Vital output status is verified every 50 ms.

Information is also passed to and from local or office code systems via the CSEX and Non-Vital I/O boards. The CPU II board controls the main system bus over which the VRD, CSEX, VSC and I/O bus interface boards communicate.

Each CPU II board contains a microprocessor to carry out VPI logic, timing, and data handling functions. By using a VT-100 Emulator, the VPI memory can be viewed and system diagnostics can be performed.

The CPU II board has the following features:

- Automatic Hardware Reset and Watchdog Timer
- Integrated Diagnostics
- Software Revision and Site ID Signature
- Polynomial Dividers
- Flash Memory for On-Board Programming
- Main Processor for Vital Processing
- Maintenance Indications
- Logic Voltage Monitoring

The group -02 version of the CPU II board also contains a second microprocessor that allows multiple VPI II systems to communicate vitally with each other. A VPI II may communicate vitally with up to 40 other VPI II systems and non-vitally to the Alstom MMS.

This group -02 board has the following additional features:

- Two USB 1.0/2.0 Controllers and Type B Connectors
- Two 10/100 Base-T Ethernet Network Controllers
- Communication Processor for Ethernet Network Interface
- EEPROM for MAC Address Storage

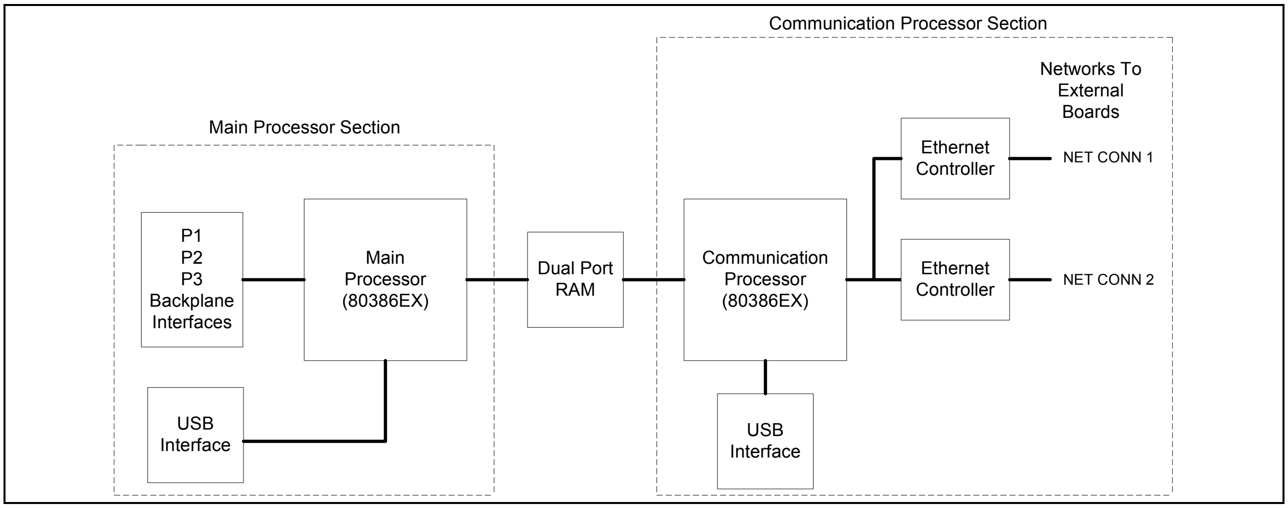

Figure 2–2. CPU II Board Block Diagram

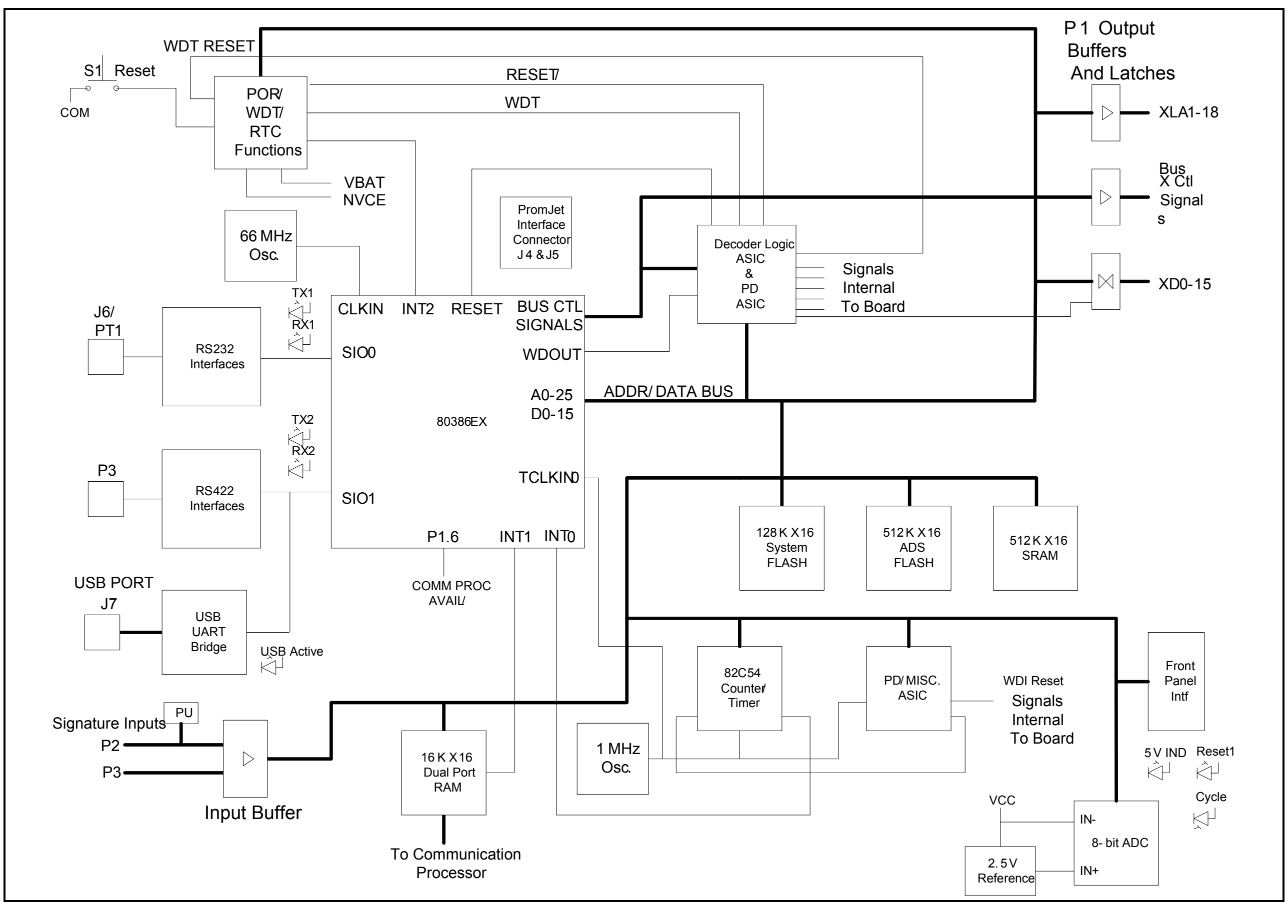

Figure 2–3. CPU II Board Main Processor Block Diagram

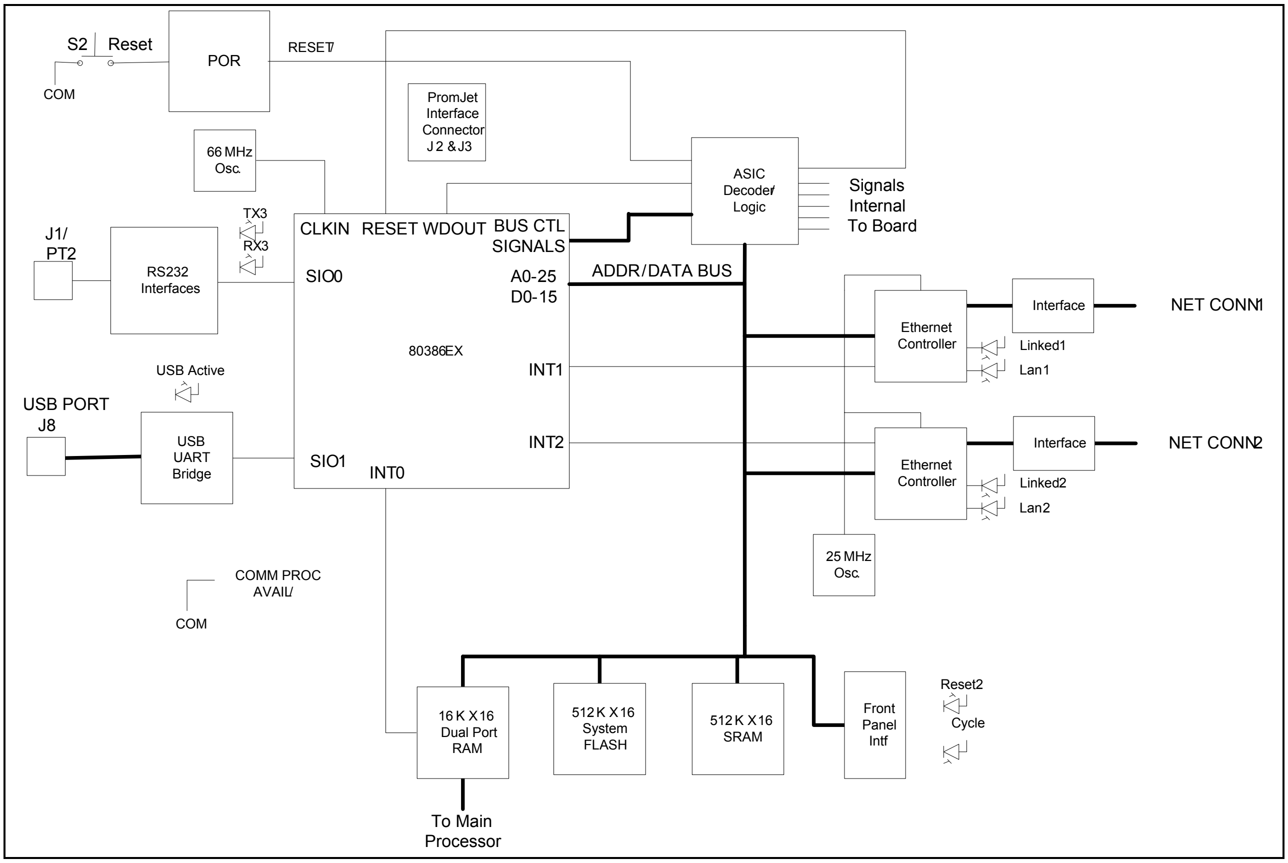

Figure 2–4. CPU II Board Communication Processor Block Diagram

2.5. OPERATION

The Main Processor performs VPI timing and data handling functions for the VPI System. The Communications Processor (only part of the -02 version of the board) performs network communication processing and interchanges data with the Main Processor via a dual-ported RAM device.

2.6. MEMORY ADDRESS DECODING

Program memory includes:

- CPU II Task (VPI Vital System Software), Two 29F010 Flash
- Application Data (VPI Application Data Structures), Two 29F040 Flash
- Communications (System Software and Application Data), Two 29F040 Flash, on group-02 boards only

These six Flash devices are socketed PLCC devices that allow for on-board programming and external programming using a separate PROM burner.

2.7. INTEGRATED DIAGNOSTICS

Within the programming memory is a system diagnostic program that tests the operation of the CPU II board and, in addition, the functional operation of most other peripheral boards by choosing different diagnostic routines. Diagnostic software is run on-line. Most parameters generated during the controlling of an application are accessible in real time. In addition, error information is displayed to the user with any of the following:

- AlsDload
- MMS (Maintenance Management System)
- VT100 emulator connection via EIA232 port or USB port
- The VDP in a CSEX board

2.8. CONFIGURABLE SYSTEM IDS

The CPU II provides a 6-bit revision signature and a 10-bit site ID for configuration control purposes. These fields can be used separately or can be combined as a 16-bit system ID. A wire table is generated as a report from the CAAPE for configuring these inputs.

2.8.1. Application Revision Signature

On the Motherboard connector and on the P3 connector for the CPU II board, six programmed binary inputs are provided. These inputs can be programmed to 5V COM to yield a binary representation of a decimal number from 0 to 63. This number corresponds to the revision number of the current application data in the CPU Flash. When the application is changed, the user can change this number via CAAPE.

2.8.2. Site ID

On connector P3 for the CPU II board, ten programmed binary inputs are provided. These inputs can be programmed to 5VCOM to yield a binary representation of a decimal number from 0 to 1023. This number corresponds to the site ID of the VPI II system. A unique number can be assigned to each system for a customer.

2.9. INDICATIONS

LED indications are located on the CPU II board's front edge to indicate board functions. Figure 2–5 shows the board edge with indications.

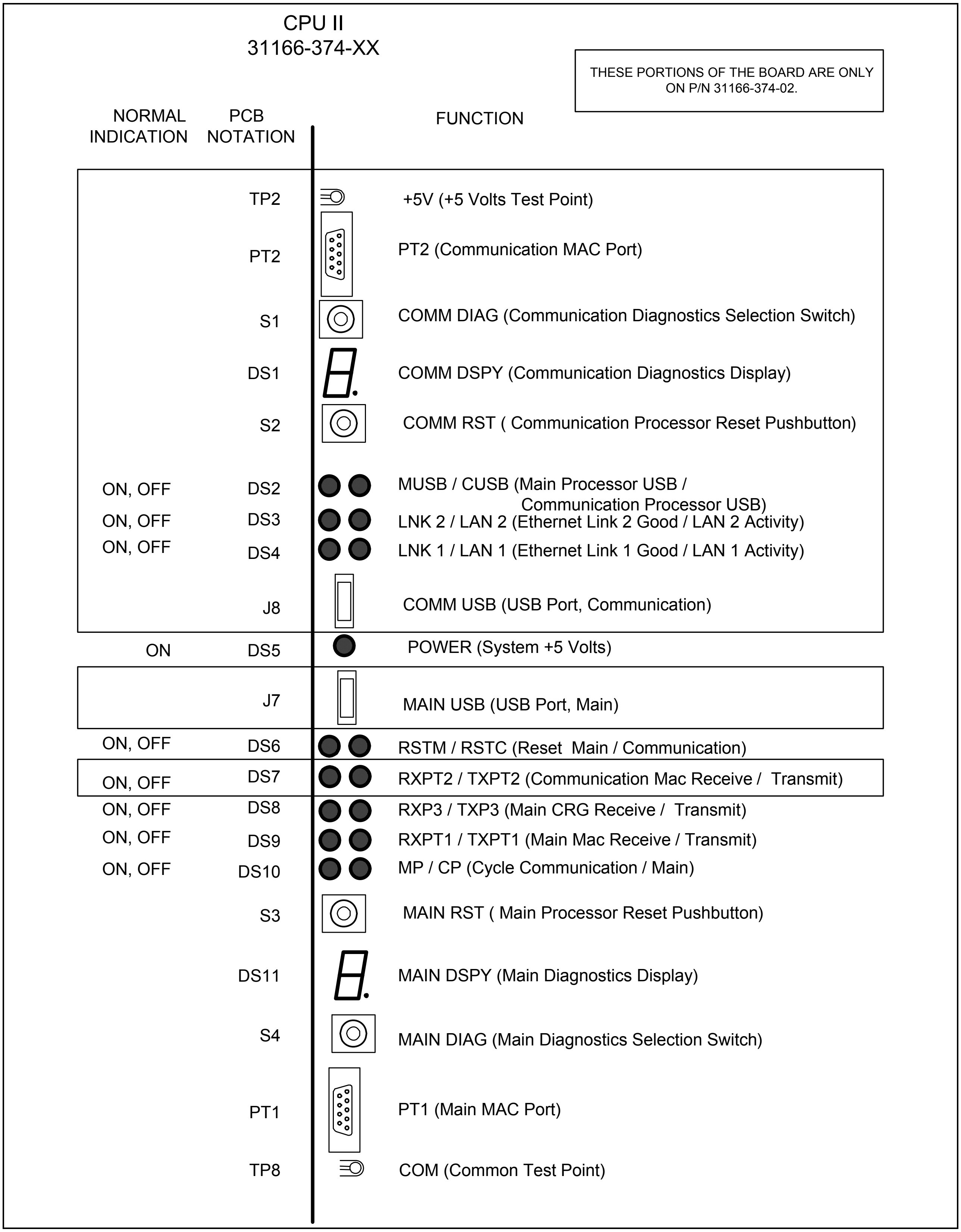

Figure 2–5. CPU II Board Edge

2.10. TEST POINTS

Table 2–2 describes the test points on the CPU II board. Oscilloscope and clip leads may be temporarily attached to the board using the test points. TP2 and TP8 are always accessible, even when the board is in a system. See Figure 2–6 for an illustration of the CPU II board including test point locations.

Table 2–2. CPU II Board Test Points

Test Point	Connection
TP2	+5V, power
TP1, TP3, TP4, TP5, TP6, TP7, TP8	COM, common
TB2, TB3, TB4, TB8, TB11, TB12, TB13	Normally open, used for factory test

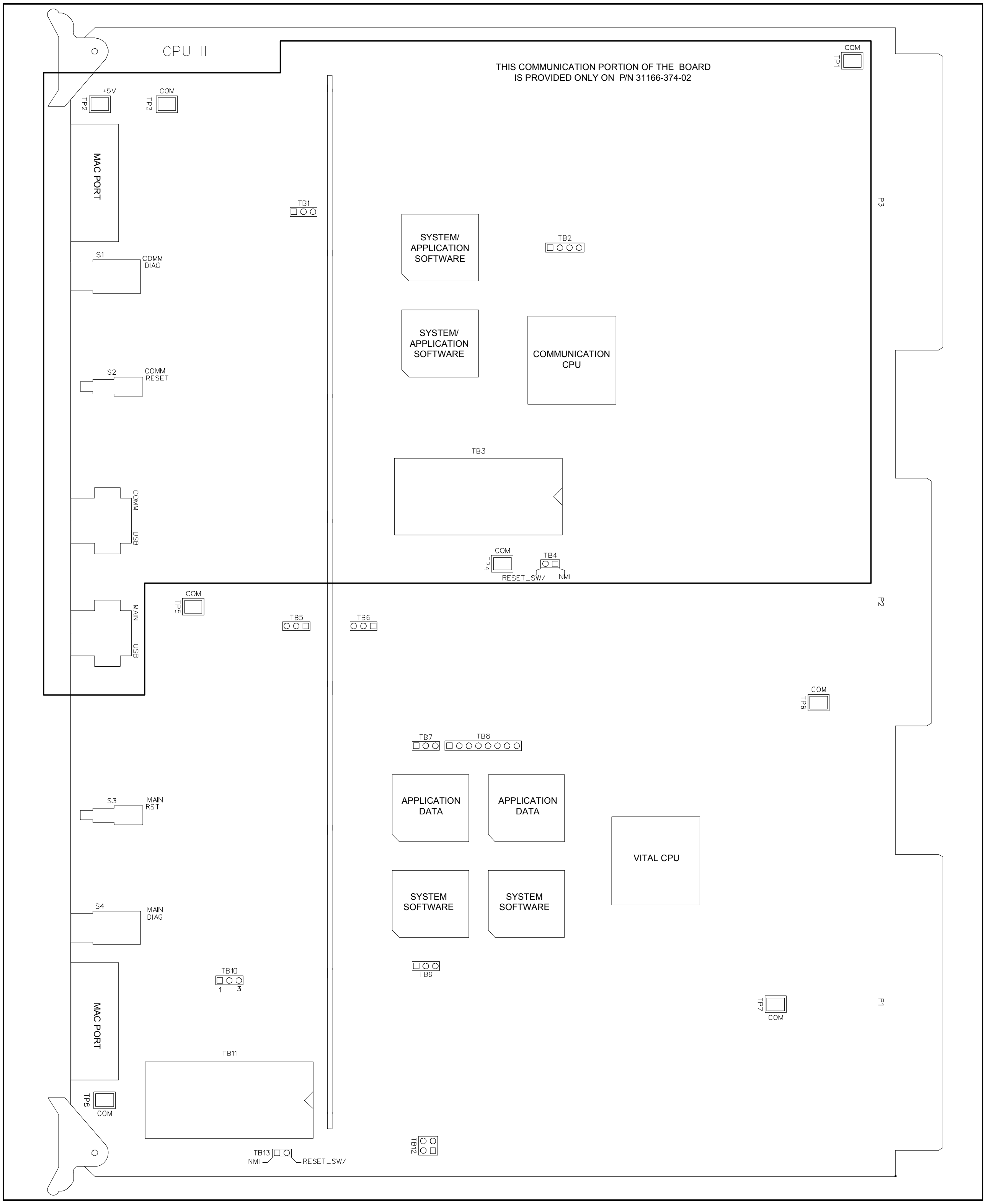

Figure 2–6. CPU II Board Test Point, Jumper, and Flash Chip Locations

2.11. JUMPERS

Tables 2–3 through 2–8 show the configurable jumper assignments for the CPU II board. All other TB locations are not user configurable. See Figure 2–6 for an illustration of the CPU II board including jumper locations.

Table 2–3. CPU II Board Battery Selection Jumper

TB5	Function
1-2	Battery disconnected (use this position for shipping and storage, or if no battery is installed during operation)
2-3	Battery connected (do not use this position if no battery is installed) (future use)

Table 2–4. CPU II Board Watchdog Selection Jumper

TB6	Function
2-3	Watchdog enabled, normal operation
1-2	Watchdog disabled (for emulator use only)

Table 2–5. CPU II Board Terminal Power Jumper

TB10	Function
1-2	VT-100 Terminal power enabled
2-3	VT-100 Terminal power disabled, normal operation for PC

Table 2–6. CPU II Main Application Flash Programming Jumper

TB7	Function
1-2	Main Application Flash On-Board Programming always enabled
2-3	Main Application Flash On-Board Programming always disabled

Table 2–7. CPU II Main System Flash Programming Jumper

TB9	Function
1-2	Main System Flash On-Board Programming always enabled
2-3	Main System Flash On-Board Programming always disabled

Table 2–8. CPU II Communication Flash Programming Jumper*

TB1	Function
1-2	Communication System Flash On-Board Programming always enabled
2-3	Communication System Flash On-Board Programming always disabled

* This jumper exists on group 2 (P/N 31166-374-02) boards only.

2.12. CARD EDGE CONNECTORS

The CPU II board (both -01 and -02) has three card edge connectors:

- P3, the top connector, is a 60-pin connector used to connect to Serial Data channel 0 and Data channel 1 of the Logic Processor; it also includes 16 input pins used to determine the system and site identification
  - See Table 2–9 for 60-pin configuration details
  - See Table 2–10 for a description of which P3 pins are used for system and site identification
  - Positions not listed in Table 2–9 or 2–10 are not user configurable
  - For CPU II group -02 boards, the P3 connector is also used to connect to the CPU II Interface Board via ribbon cable at J1 on the CPU2 Motherboard.
- P2, the middle connector, is a 50-pin connector used for system voltage and common; it also includes 6 input pins used to determine the revision identification
  - See Table 2–10 for a description of which P2 pins are used for revision identification
  - Positions not listed in Table 2–10 are not user configurable
- P1, the lower connector, is a 60-pin connector which interfaces with the VPI system bus,; this connector is not user configurable

NOTE

P2-10, P2-15, P2-22, P2-31, P2-38, P2-48 and P3-2, P3-4, P3-6, P3-8, P3-10, P3-12, P3-14, P3-16, P3-18, and P3-20 are common connections available for configuring the ID along with the connections in Table 2–10.

Table 2–9. CPU II Board 60-pin P3 Connections

P3-	Name	Function
27	COM	Backplane MMS Connection Common
29	RS232-RX	Backplane MMS Connection Receive
33	TXIA	Backplane MMS Connection Transmit
35	TX2+	Ethernet Channel 2 transmit +, group -02 board only
36	TX2-	Ethernet Channel 2 transmit -, group -02 board only
37	RX2+	Ethernet Channel 2 receive +, group -02 board only
38	RX2-	Ethernet Channel 2 receive -, group -02 board only
39	COM	Ethernet Channel 2 common, group -02 board only
40	RD1+	CRG receive +
42	RD1-	CRG receive -
49	TD+	CRG transmit +
50	TD-	CRG transmit -
51	TX1+	Ethernet Channel 1 transmit +, group -02 board only
52	TX1-	Ethernet Channel 1 transmit -, group -02 board only
53	RX1+	Ethernet Channel 1 receive +, group -02 board only
54	RX1-	Ethernet Channel 1 receive -, group -02 board only
55	COM	Ethernet Channel 1 common, group -02 board only

Table 2–10. P2 and P3 Connections Used For Revision and Site Identification

System ID Name	Rev or Site ID Name	P3 Connection	P2 Connection
ID0	Rev ID0	P3-21	P2-42
ID1	Rev ID1	P3-22	P2-43
ID2	Rev ID2	P3-23	P2-44
ID3	Rev ID3	P3-24	P2-45
ID4	Rev ID4	P3-25	P2-46
ID5	Rev ID5	P3-26	P2-47
ID6	Site ID0	P3-1	N/A
ID7	Site ID1	P3-3	N/A
ID8	Site ID2	P3-5	N/A
ID9	Site ID3	P3-7	N/A
ID10	Site ID4	P3-9	N/A
ID11	Site ID5	P3-11	N/A
ID12	Site ID6	P3-13	N/A
ID13	Site ID7	P3-15	N/A
ID14	Site ID8	P3-17	N/A
ID15	Site ID9	P3-19	N/A

2.13. ADDITIONAL CONNECTORS

Both the -01 and -02 versions of the board also include these connectors:

- Connector J6/PT1 is a 9-pin Main Processor EIA232 interface connector
- Connectors J5 & J4 are 38-pin Test Connectors for the Main Processor Databus, address bus and control signals; these are not user configurable

CPU II board -02 supports a communications interface with the following additional connectors:

- Connector J1/PT2 is a 9-pin Communication Processor EIA232 interface connector
- Connector J7/MAIN USB is a Main Processor USB Interface connector
- Connector J8/COMM USB is a Communication Processor USB Interface connector
- Connectors J2 & J3 are 38-pin Test connectors for the Communication Processor Databus, address bus and control signals; these are not user configurable

2.14. CPU2 INTERFACE BOARD (P/N 31166-499-XX)

The CPU2 Interface Board is mounted on DIN rails at the rear of the rack. It is connected to the P3 board edge connector on the CPU2 motherboard through a ribbon cable at J1.

It is used in CPU II group -02 configurations and used to provide communication and site ID features, including:

- Bit selection for the Logic Processor section of the CPU board.
- 2 RJ45 Ethernet jacks (J2 and J3) with LEDs for the Ethernet channels on P3 of the CPU2 motherboard.
- 1 RJ45, without LEDs, designated for serial data transmission, PrPT1_RXD and PT1_TXD.
- 1 RJ25 for the +/- COMM_PROC_ALIVE signal to be recognized.

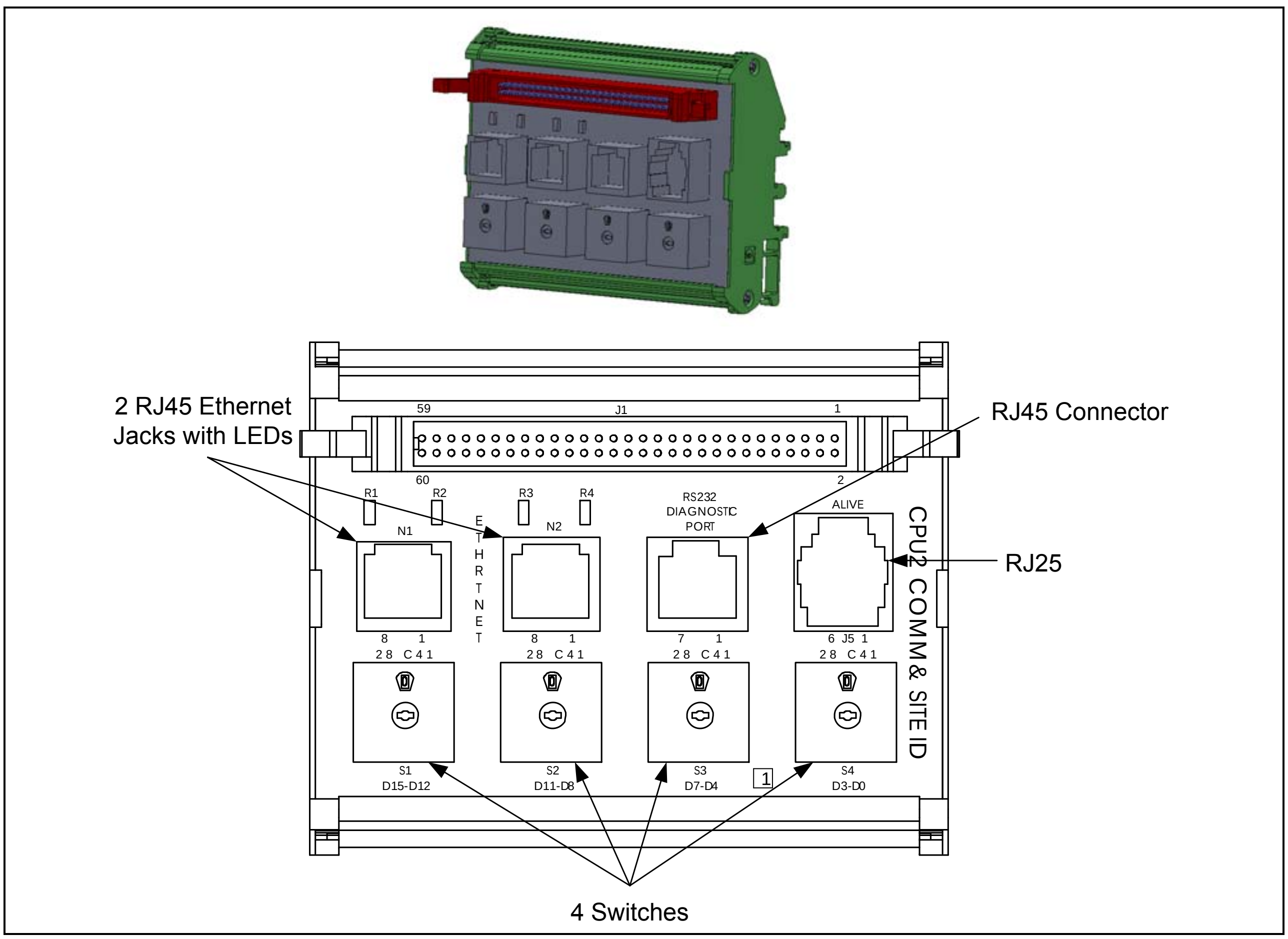

Figure 2–7. CPU2 Interface Board

2.14.1. Logic Processor Bit Designations

CPU2 Interface Board switches S1-S4 control the System ID selection for the Logic Processor section of the CPU board. These inputs can be programmed to 5V or common to provide a binary representation of a hexadecimal number from 0-63. This number corresponds to the revision identification (Site ID and Revision ID) of the current application in the CPU FLASH. When the application is changed, the CAA changes this number in the FLASH memory. The hardware must be reprogrammed to tie a particular CPU board to a specific application. Programming is completed by setting switches S1 through S4 appropriately. Figure 2–8 shows the appropriate system ID designations (x3 = S1, x-2 = S2, x1 = S3, x0 = S4; Most Significant Bit – Least Significant Bit).

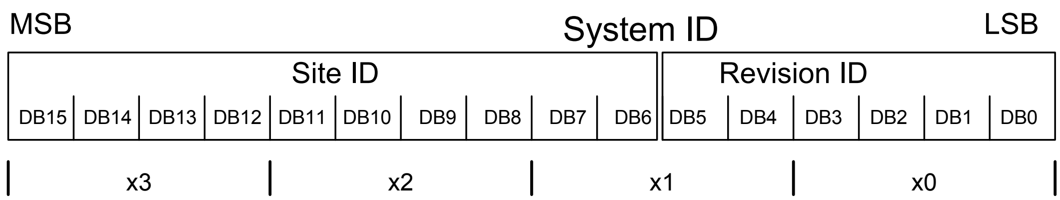

Figure 2–8. CPU2 Interface Board Logic Processor System ID Designations

2.15. SPECIFICATIONS/ASSEMBLY DIFFERENCES

Table 2–11. CPU II Board Specifications/Assembly Differences

Specifications	**31166-374**	
	-01	**-02**
Maximum Number of Boards Per VPI II System	1	
Board Slots Required	1	
Maximum Board Logic Current Supply	1.5A	
Supports 29F010 Flash	Yes	
Supports 29F040 Flash	Yes	
VPI CAA Version	-050 and later	-100 and later
Ethernet Communications	No	Yes
Supports USB	No	Yes

3. SECTION 3 – VRD (VITAL RELAY DRIVER) BOARD, P/N 59473-740-02

3.1. INTRODUCTION

This section provides VRD board detail.

3.2. GENERAL

Figure 3–1 shows a block diagram of the Vital Relay Driver (VRD) board. This board plays a key role in assuring the vitality of the system. It produces an output voltage capable of operating a 100Ω Alstom Type B relay (56001-787-05) if, and only if, the data sent to it by the main processing system is correct. The main processing system creates a set of data called “main checkwords” once every second. These checkwords are used by the VRD board. They allow it to continue operation for another 1-second period. In addition, the main processing system generates a set of recheck checkwords every 50 ms based on the status of all the system’s outputs. These checkwords are sent to the VRD board every 50 ms where they are used to produce 50 ms worth of output. If any of these checkwords are not precisely correct, the VRD output is shut off and the external relay de-energizes.

3.3. OPERATION

The processing portion of the VRD board is based on an 8085 microprocessor chip with 4K of EPROM program memory and 4K of RAM. The RAM is shared with the main processing system and is the means by which the checkwords are transferred from the CPU II board to the VRD board.

Once every second the main processing system delivers a new set of data called main checkwords to the VRD board. The VRD board processes these main checkwords and converts them to “tokens.” The VRD requires 20 tokens to operate for the next one-second period. Every 50 ms the main processing system delivers a set of data called “recheck checkwords” to the VRD. The VRD uses one token and the set of recheck checkwords to create an output signal for 50 ms. If any of the checkwords is incorrect or if the new checkwords are not delivered on time, the VRD output is lost.

The output of the processing portion of the VRD board (when all checkwords are correct) is a 10 kHz square wave modulated at 500-Hz. This signal passes through a 10 kHz tuned circuit and then a 500-Hz tuned circuit. The output of the 500-Hz tuned circuit is rectified and filtered to produce an isolated DC voltage to energize an Alstom Type B 100Ω relay. Front contacts of this relay or its repeater(s) are used to feed output power to the Vital output boards. When the isolated DC voltage is removed and this relay drops, all Vital outputs of the system are de-energized.

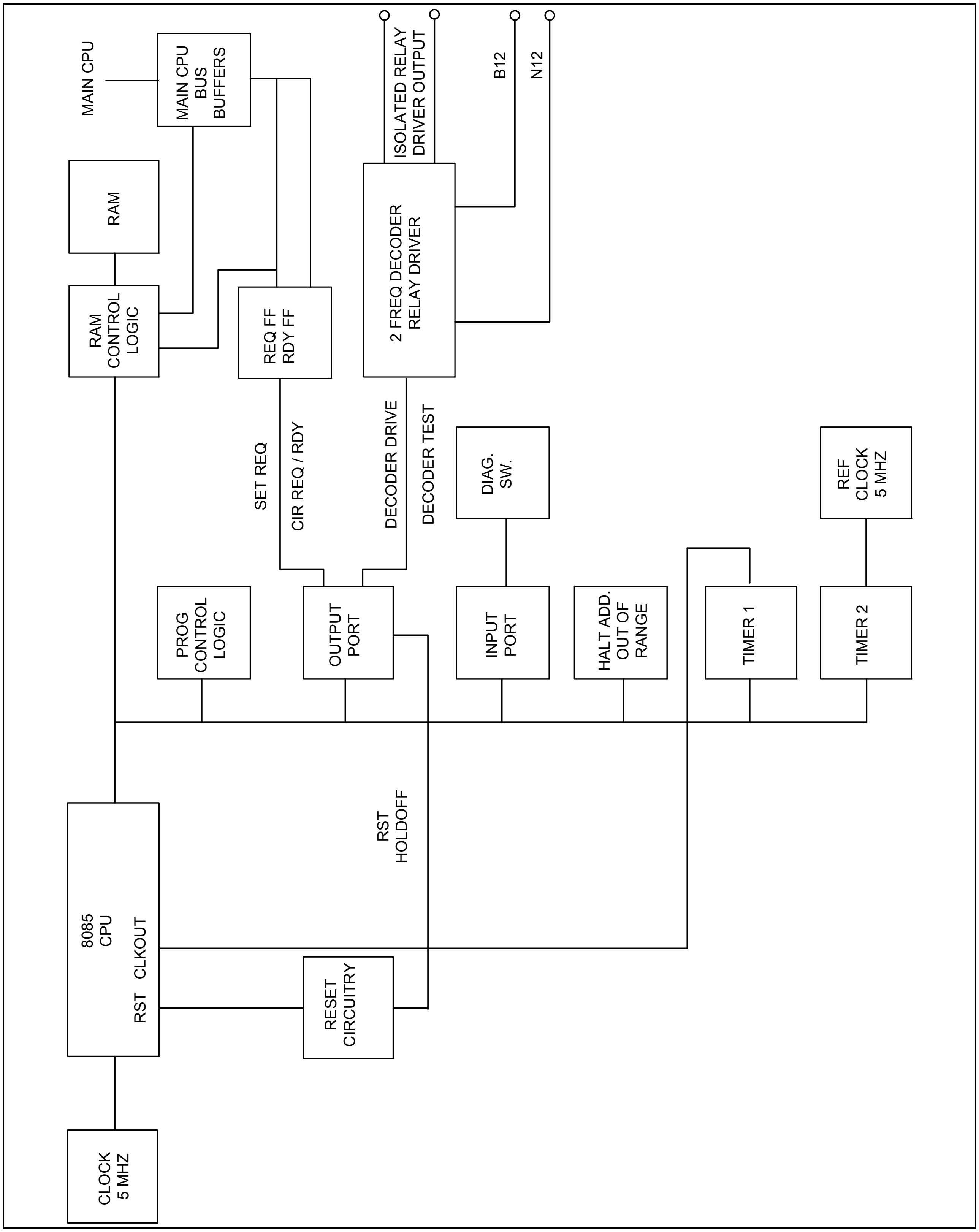

Figure 3–1. VRD Board Block Diagram

The VRD board gives the main processing system three chances to deliver the new checkwords before shutting down the outputs. This is to allow for clock variations and variations in system timing. As part of the recheck checkword set, three dummy checkwords are sent to the VRD. These three checkwords cause the VRD to look for a new set of checkwords. The VRD creates a 46 ms output if the set of recheck checkwords it received is correct. It then creates an additional 2 ms output, using the first of the dummy checkwords. However, during a portion of this period, the VRD allows the main processing system to deliver a new set of checkwords. If the main processing system does not deliver the new checkwords, then the VRD uses the second dummy checkword and tries again 2 ms later. If it still does not receive the new set of checkwords by the third try, it has run out of checkwords and no longer produces the proper output.

The VRD program uses Safety Assurance Logic that does not change from system to system and cannot produce the correct output without the checkwords being correct. The VRD requires that the checkwords received from the main processing system be different on each cycle.

3.4. STATUS OR ACTIVITY INDICATORS

This board has three LED indicators for use as troubleshooting aids, as shown in Figure 3–2. The top indicator illuminates whenever the signal produced by the processing portion of this board passes through the 10 kHz tuned circuit. The remaining two indicators illuminate during the exchange of handshaking controls between the VRD board and the main processing system. These controls are REQ/ and RDY/. During normal operation, each of these indicators turns on or off each time that their respective control line changes state. Depending upon system timing, one of these indicators may appear to be on all the time while the other appears to be off most of the time or these LEDs may appear to flash alternately. If neither indicator flashes, then it means the main processing system and the VRD are not communicating with each other.

A 16-position control switch is located along the front edge of this board. This switch must be set to position F to allow the system to attempt a restart if the VRD relay de-energizes. As part of the restart procedure, the board runs a 7-second delay before it accepts any checkwords from the main processing system. If the processor halts or tries to operate in memory locations outside the allocated memory space, it is automatically reset. The system removes power from the outputs immediately in the event of a failure.

NOTE

> If the control switch is in any position other than F, the system does not attempt to restart.

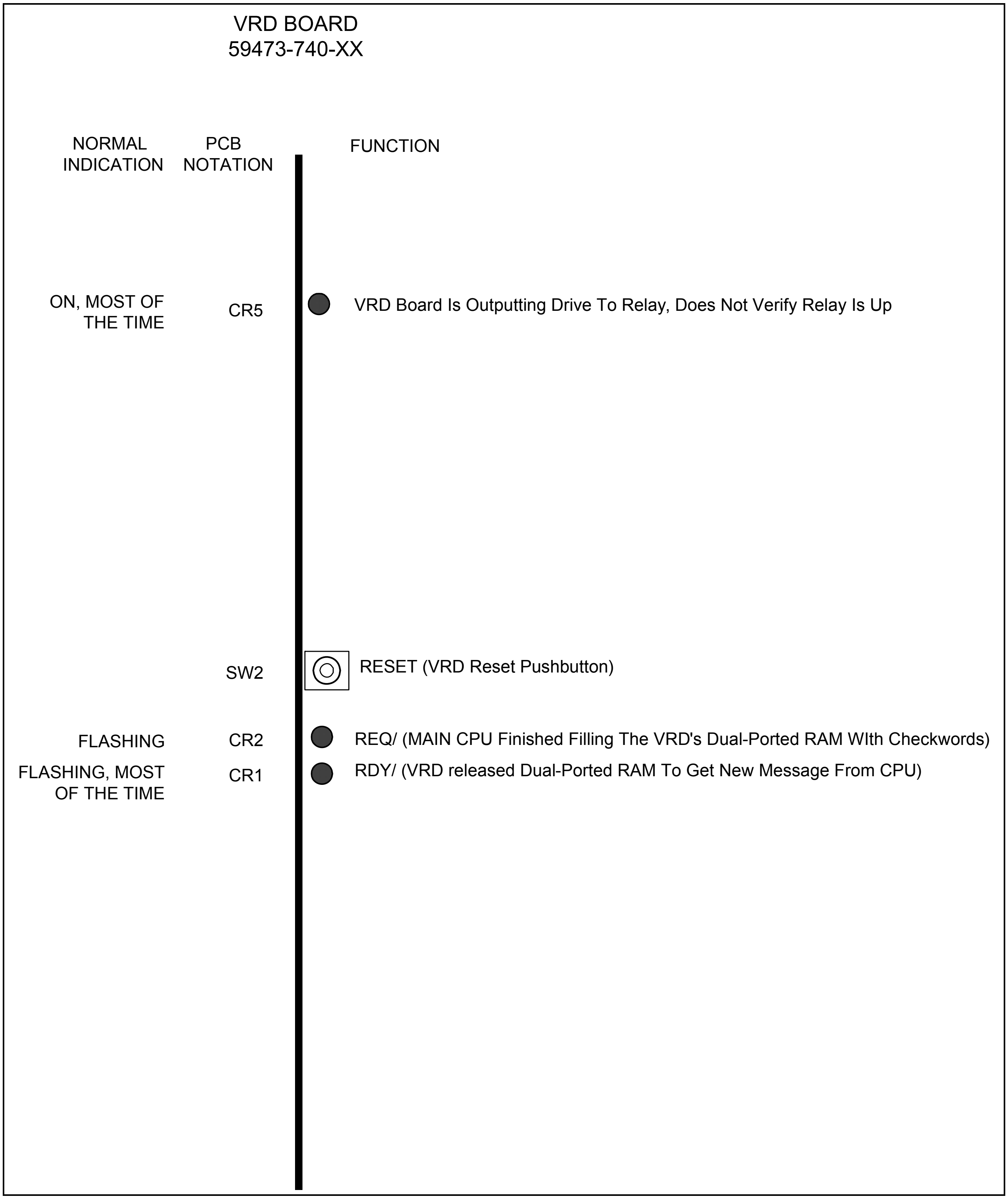

Figure 3–2. VRD Board Edge

3.5. TEST POINTS

See Figure 3–3 for the VRD board test point locations.

Table 3–1. VRD Board Test Points

Test Points	
TP1, TP2, TP3, TP4, TP5	used for factory test

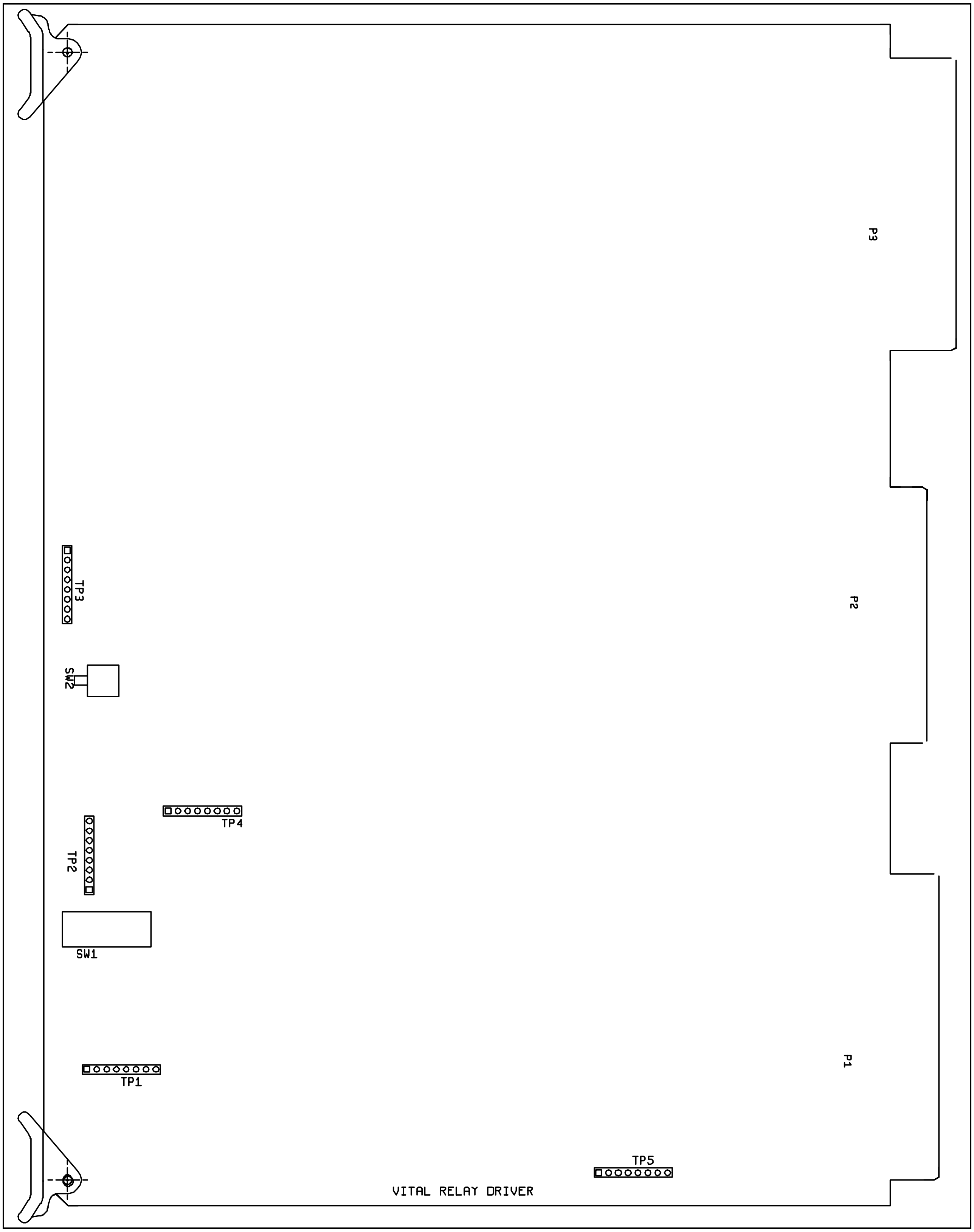

Figure 3–3. VRD Board Switch and Test Point Locations

3.6. SWITCHES

See Figure 3–3 for the VRD board switch locations and Figure 3–4 for the VRD board SW1 switch setting.

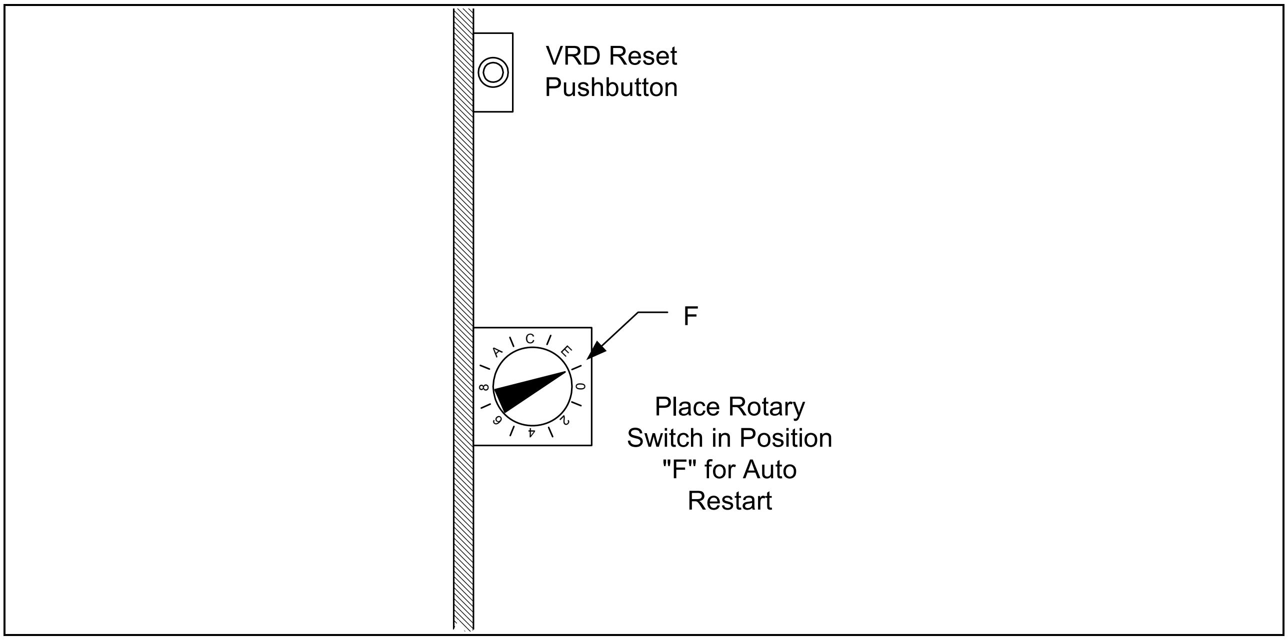

Figure 3–4. VRD Board SW1 Switch Setting

3.7. CARD EDGE CONNECTORS

The VRD board has three card edge connectors:

- P3, the top connector, is a 36 -pin connector used to interface to the Vital energy disconnect relay
  - See Table 3–2 for power connection pins details; the remaining P3 pins are not user configurable
- P2, the middle connector, is a 50 -pin connector used for system voltage and common
  - P2-43 through P2-47 are wired in a specific pattern to common P2-48 per the application .lvc CAAPE report for board addressing; the remaining P2 pins are not user configurable
- P1, the lower connector, is a 60-pin connector that connects to the system bus; this connector is not user configurable

Table 3–2. VRD Board P3 Power Connections

P3-	Name	Function
3	-OUT	Relay Coil -
6	+OUT	Relay Coil +
32	12VCOM	Common
36	+12V	12 Volt +

3.8. SPECIFICATIONS

Table 3–3. VRD Board Specifications

Specification	59473-740-02
Maximum Number of Boards Per VPI System	1
Board Slots Required	2
Maximum Board Logic Current Supply	300 mA
VRD Drive Output Isolation	>3000 Vrms
Minimum VRD Supply Voltage	9.00 VDC
Maximum VRD Supply Voltage	15.00 VDC
Typical VRD Drive Current Draw @ 12.00 V	40 mA

4. SECTION 4 – VSC (VITAL SERIAL CONTROLLER) BOARD, P/N 59473-939-XX

4.1. INTRODUCTION

This section provides VSC board detail.

4.2. GENERAL

The Vital Serial Controller (VSC) board is a microprocessor-based board that provides a means for exchanging the states of up to 200 Vital interlocking functions (in each direction) between interlocking systems in a Vital manner. This communication is used between Vital systems within the train control room and from room to room for limited distances.

This board family was first designed to provide VPI to VPI Vital communications more efficiently than line wires. There are two types of data transmission interfaces; one for private copper pairs and one for generic, EIA232, DCE connection. A daughter board is used to provide the EIA232 connection, so the number of chassis slots required for this interface board is two (2).

Two additional applications of the VSC were created to provide a means of communicating to and from

- VPI and AF Track Circuit modules (MVSC)
- VPI and Programmable Genrakode modules (GVSC and GVSCE)

The system software installed on the Vital Serial Controller board is associated with a particular version of system software on the CPU II board. Each type of board, MVSC, GVSC, or VSC, has its own unique Vital system software that is not interchangeable, see Table 4–7 VSC Board Specifications.

When used for MVSC up to 450 Vital parameters can be transmitted in each direction. The GVSC sends and receives up to 30 Vital parameters of information in its messages to each of a maximum of two Genrakode modules. Up to ten VSC boards or combinations of VSC, MVSC, GVSC, GVSCE, CRG (Code Rate Generator), and CSEX boards can be supported by a single Vital subsystem.

The application software is programmed with CAAPE, generating programs for EPROMs (EPROM U18 P/N 01169-646-ON) for the up to ten VSC boards mentioned above.

4.3. OPERATION

The VSC is a VPI II system board that resides on the VPI system bus. Link information, in the form of system parameter values and checkwords, is provided from the VPI CPU system RAM over the system bus to dual-ported RAM (DPRAM) memory on the VSC. The block of data, or message packet, is then moved under VSC control to the transmit processing RAM memory.

The transmit process converts message packet contents into two serial message components; an image field and a check field. The image field represents the true/false (or permissive/non-permissive) state of each system parameter in the provided message block. The check field incorporates a combination of all link processing checkwords created up to this point in the link transfer. These fields, plus transmit/receive protocol flags, are formed into a Synchronous Data Link Control (SDLC) protocol-like message and transmitted. SDLC is a simplified data transmission protocol developed by IBM designed to optimize transmission of data bits.

The receive process uses the image field to reconstruct a receive message packet with parameter values resembling those passed from the CPU II board to the VSC board at the transmit end. This reconstructed block of data, along with a receive link checkword, is passed to the CPU upon request. The receive link checkword includes all link checkwords created along the data path to this point.

4.4. COMMUNICATION

There are multiple versions of the VSC board:

- VSC board providing communication between two VPI II Systems
- MVSC board providing communication between a VPI II and an AF Track Circuit Module
- GVSC board providing communication between a VPI II and Programmable Genrakode (PGK)
- GVSCE board providing communication between a VPI II and Programmable Genrakode (PGK); this board supports 50 Vital parameters returning from each module, up to 25 parameters for each track; the other VSC board types support 30 Vital parameters/15 from each track

Each type of board, MVSC, GVSC, GVSCE or VSC, has its own unique Vital system software that is not interchangeable and must be matched with specific versions of the CPU II system software. The basic difference in the system software is the message structure used by each board. The MVSC, GVSC or GVSCE transmits a message containing 450 Vital parameters that is sent simultaneously to the various addressable AF modules or PGK boards on the serial line. It then listens for responses from the modules, with 30 (50 for GVSCE) Vital parameters returning from each module. The VSC, used for VPI-to-VPI communications, sends and receives up to 200 Vital parameters of information in its message.

NOTE

In the descriptions that follow, the term VSC is used generically to describe a Vital serial communication board of any of the types (MVSC, GVSC, GVSCE or VSC).

4.4.1. VSC Board, VPI to VPI Communication

One version of the VSC board is used to provide Vital serial communication from VPI-to-VPI via a transformer coupled, proprietary communications protocol (P/N 59473-939 -10, -17) over two twisted pairs. When using appropriate cable, it is possible to communicate reliably over distances of four miles.

To communicate from one train control room to another over the fiber optic system, a different assembly version of VSC board is used. This VSC board (P/N 59473-939-11, -18) contains a special interface board (P/N 31166-058-01), referred to as a "daughter board", that is mounted on the VSC board itself. This daughter board contains an EIA232 converter that allows the VSC board to interface directly with compatible line cards in T1 multiplexers and other standard communications equipment that may be part of an existing copper or fiber optic data transmission system.

CAUTION

> When planning to use a data communications backbone to pass VSC messages between interlockings, confirm that the backbone protocols are able to deliver the complete message at the receiving end in 400 milliseconds.
>
> If the reception exceeds 400 ms, all the message parameters are forced false.

4.4.2. VSC Board, VPI to AF Track Circuit Module Communication

Another version of the VSC was created to provide a means of communicating to and from AF Track Circuit modules. This Multi-Drop Vital Serial Controller (MVSC) board is capable of communicating by using vitally addressable destinations. Up to 15 AFTC modules may be multi-dropped on one serial line. The MVSC board (59473-939-12) hardware and operation are almost identical to the VSC.

4.4.3. GVSC Board, VPI to Programmable Genrakode (PGK) Board Communication

A different multi-drop version of the VSC is the Genrakode Vital Serial Controller (GVSC) board. It is capable of communicating with up to two Programmable Genrakode (PGK) boards on a 2-wire half-duplex line. This application allows for the communication of up to 15 parameters for each track. The GVSC board (59473-939-13) hardware and operation are almost identical to MVSC.

4.4.4. GVSCE Board, VPI to PGK Board Communication

Another multi-drop version of the VSC is the Genrakode Vital Serial Controller Extended (GVSCE) board. It is capable of communicating with up to two Programmable Genrakode (PGK) boards on a 2-wire half-duplex line. This version allows for the communication of up to 25 parameters for each track. The GVSCE board (59473-939-14) hardware and operation are almost identical to GVSC and is required when a full implementation of Code T™ is needed.

4.5. COMMUNICATION PROCESS

The VSC is a system board that must reside on the VPI System bus. Link information in the form of system parameter values and checkwords is provided from the VPI CPU system RAM over the system bus to Dual Ported RAM (DPRAM) memory located on the VSC. The block of data (or message packet) is then moved, under VSC control, to the transmit processing RAM area.

The transmit process converts message packet contents into two serial message components: an “image field” and a “check field.” The image field represents the TRUE/FALSE (or PERMISSIVE/NON-PERMISSIVE) state of each system parameter in the provided message block. The check field incorporates a combination of all link processing checkwords created up to this point in the link transfer. These fields, plus transmit/receive protocol flags, are formed into a message and transmitted.

The receive process uses the image field to reconstruct a receive message packet with parameter values resembling those passed from the CPU II board to the VSC board at the transmit end. This reconstructed block of data, along with a receive link checkword, are passed to the CPU upon request. The receive link checkword includes all link checkwords created along the data path to this point.

The CPU then retrieves the input message packet from the VSC DPRAM and places it in its input matrix. Processing is performed to combine the receive end CPU link checkwords with those provided from the VSC board. If all checkwords are correct and the path of the data is correct (e.g. origin in SYSTEM 1 CPU to destination in CPU of SYSTEM 3), parameters directed to be in a TRUE state by the transmit end are allowed to assume the correct TRUE parameter value within the receive end CPU memory. Otherwise, failures along the link path have occurred and all link parameters are forced into a FALSE (restrictive) state. These parameters are subsequently used as required during expression evaluation at the receiving end.

A maximum of ten VSC boards may be used in a VPI system supported by CAA 31746-025 and later. These may reside in both the SYSTEM MODULE and EXPANSION MODULE. The maximum number is dependent on the number of CRG and CSEX boards being used.

4.6. MEMORY TYPES

The VSC program and application memory is designed to be one of two types; 16K or 32K × 8 bits, which is DIP switch selectable (SW4) board functions allocated to SW4 are shown in Figure 4–8.

NOTE

Only the 16K x 8 bit memory size is currently supported.

4.7. STATUS AND ACTIVITY INDICATORS

Eleven LED indicators are provided on the VSC. Eight are multipurpose indicators for use with diagnostic software. Another indicator is assigned as a power supply voltage level monitor. An output of the watchdog timer IC drives the LED when the VSC board supply is below 4.6 VDC. Another indicator illuminates when the VSC is in a reset condition. A final indicator driven by the SCC (Serial Controller Chip) is used to display serial link activity. Refer to Figure 4–1 for an illustration of the VSC board edge.

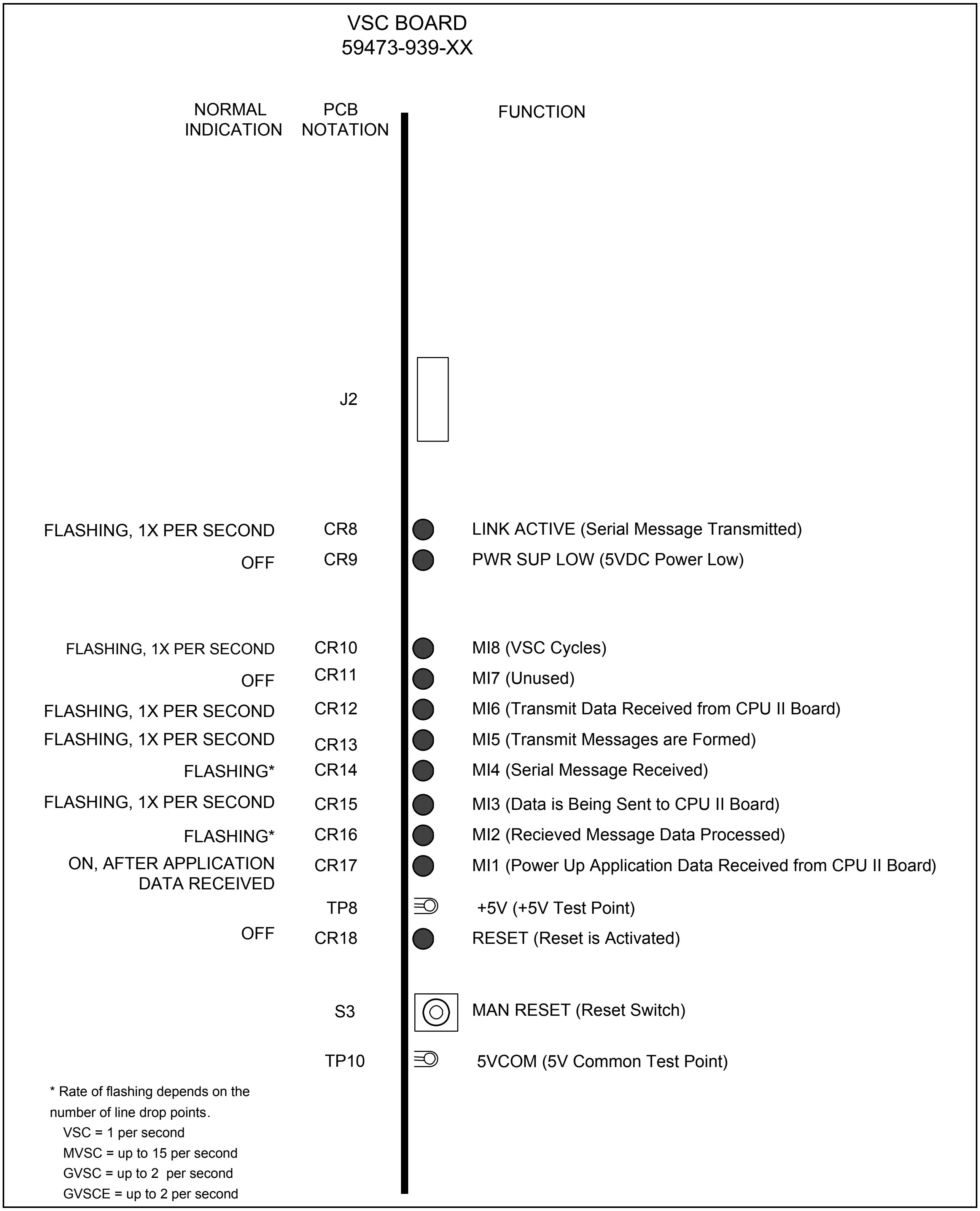

Figure 4–1. VSC Board Edge

4.8. COMMUNICATION INTERFACES

There are two different physical communications interfaces available in this board series. A direct wire interface that requires two copper pairs and an industry standard EIA232 signal level interface for use with data communications equipment. The choice of interface is primarily an economic one, the Vital operation of the VSC link is not altered by the choice of physical interface. However, reliability of the communication link may be affected depending upon the choice made and the electrical environment.

4.9. DIRECT WIRE INTERFACE

4.9.1. Serial Communication Controller - Manchester Encoder-Decoder

The VPI-VPI link is controlled by one channel of a serial communications controller (SCC) IC (82530 or 85C30). Data is provided to and from the SCC under interrupt control. Its output and input data is converted between non-return-to-zero (NRZ) and Manchester format by a Manchester encoder/decoder (MED) device (6409). Data is provided in synchronous mode. Synchronous data link control (SDLC) format is used for this link interface.

4.9.2. Serial Link Interface

The VSC contains a full duplex interface for linking VPI-to-VPI. Baud rate is 19.2 K for standard applications. The serial data stream is converted from NRZ to a Manchester coding format. This format is such that each data bit cell contains a logic transition. Therefore, a continual stream of logic ‘0’ data bits is not a constant signal level but rather a series of cycles each with a low to high transition in the center of the data bit. Similarly, a continual stream of logic ‘1’ data bits has a high to low transition in the center of the data bit interval. Refer to Figure 4–2 for a comparison between NRZ and Manchester encoding. This signal is twice the frequency of the data bit stream provided by the USART. The advantage of this data format is that due to its continuous transitions, the signal can be used to power a transformer without a DC component. The Manchester Encoder/Decoder also provides the benefit of message synchronization, clock recovery and noise immunity.

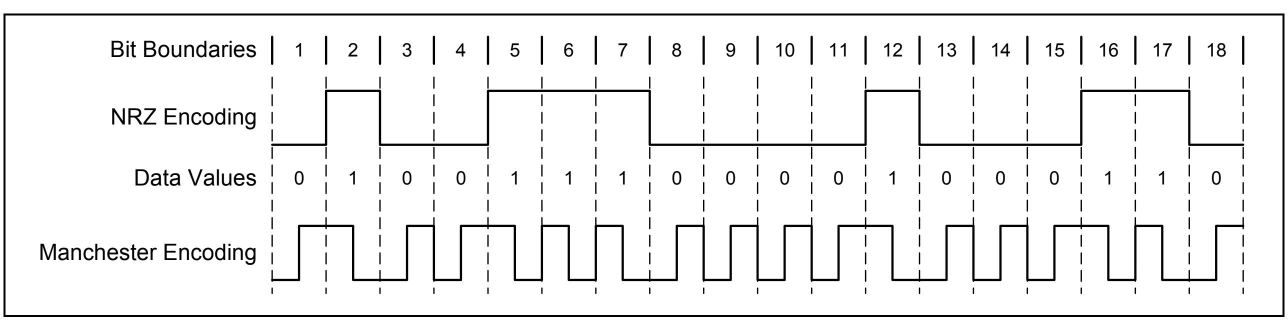

Figure 4–2. The Effect of Manchester Encoding on NRZ Data

4.10. DATA TRANSMISSION

The signal supplied by the MED is provided to an EIA422 driver. The EIA422 driver drives a transformer in differential mode. The voltage swing of the driver is 4 Vp-p (typical).

The transformer interfaces with twisted pair communication links having a characteristic impedance of about 100Ω at a signal frequency of 19.2 kHz. It provides isolation of the system 5V supply from external references. The transformer has a center-tapped secondary that allows for a 1:1 or a 1:2 turns ratio. For the transmit direction the 1:1 configuration is used. The VPI-VPI link uses two transformers for full duplex operation. The receiver transformer uses the 1:2 transformer configuration to step up the incoming signal.

Jumpers in the transformer secondary can be used to modify the turn's ratio later if necessary. The secondary of the transformer interfaces with the twisted pair link via a line termination, transient suppression and low-pass filter network. A 100Ω resistor terminates the twisted pair link in its characteristic impedance to minimize line reflections. Back-to-back transient suppressors clamp the link at 12V in either polarity. The L-C low-pass filter in each leg of the link has a cutoff frequency of 100 kHz. This filter arrangement provides common mode and differential mode filtering. Also, 68 uH inductors serve as series resistive elements with the transient suppressor to limit current surges.

4.11. DATA RECEPTION

The VPI-VPI link receiver section uses the same transformer as the transmitter but converts the 4Vp-p signal to an 8 Vp-p on the secondary side that feeds the EIA422 differential receiver. The EIA422 receiver output provides a 5V logic representation of the differential signal to the MED. In the receive circuit, resistors provide hysteresis to minimize the effect of interference on the message data. The receiver responds to receive signals > ± 800 mV.

4.12. APPLICATION WIRING

The VSC uses a transformer-coupled twisted pair link as the medium of data exchange. Serial link transmission distances of up to four miles are possible given that a suitable variety of twisted shielded cable is used and cable runs are separated from high power transmission cables. The recommended minimum conductor size to achieve the four mile distance is 16 AWG. Primary lightning protection is necessary for link runs that are accessible to lightning strikes, e.g., aerial runs, above ground duct banks, etc. The protection should be located as close to where the cable enters the house as practical.

The recommended cabling scheme for the VSC link is shown in Figure 4–3. Shielded cable is not required for all installations. However, if shielded cable is used, the shield must be connected to earth ground at only one point. This point need not be at the same location as one of the two VPI systems. If a better ground is available at some other point on the cable run, e.g., a junction box, the shield may be grounded at that point.

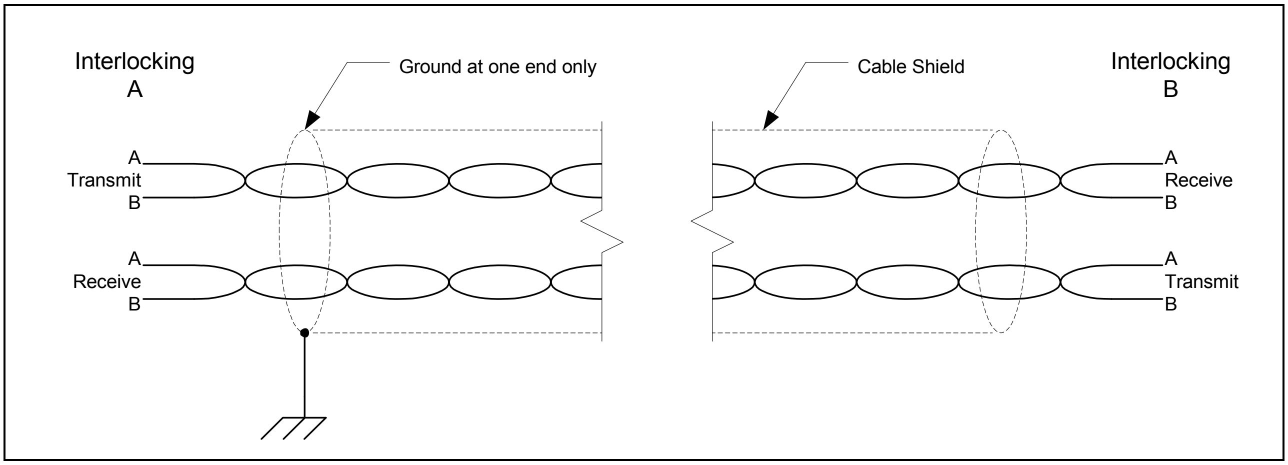

Figure 4–3. VSC Link Cable and Shield Connections

4.13. DATA COMMUNICATIONS INTERFACE

The data communications interface is provided through the addition of a daughter board. The daughter board, P/N 31166-058-01, provides a galvanically isolated interface (optical) to the data communication equipment. This reduces the likelihood that circulating currents in possible ground loops with other equipment effect the operation of the VPI electronics. See Figure 4–10 for the layout of the daughter board.

WARNING

WHEN USING ASSEMBLY VERSIONS THAT INCLUDE THE DAUGHTER BOARD AN EXTERNAL POWER SOURCE MUST BE PROVIDED. THIS ENERGY SOURCE MUST NOT BE A VITAL ENERGY OR A NON-VITAL ENERGY THAT CANNOT BE CONNECTED TO EARTH GROUND. THIS IS BECAUSE THE COMMUNICATION EQUIPMENT THAT THE DAUGHTER BOARD CONNECTS TO USUALLY CONNECTS SIGNAL COMMON, FOR EXAMPLE ISOCOM, P3-36 (PLUG COUPLER H1), TO EARTH GROUND.

4.14. DATA TRANSMISSION AND RECEPTION

When the daughter board is installed on the VSC board, it establishes connections to the SCC serial data lines and the connections that the SCC had to the Manchester encoder-decoder are severed. The message format is changed from synchronous to asynchronous. The asynchronous message format is one start bit, 8 data bits, no parity bit and two stop bits. The data transmission rate may be at either 9600 or 19200 bits per second. The data communication equipment used with this interface must be able to support this format.

WARNING

THE FEATURES AND CAPABILITIES OF THE DATA COMMUNICATION EQUIPMENT MUST BE CAREFULLY REVIEWED TO INSURE THAT ANY MESSAGE BUFFERING OR ERROR CORRECTING PROTOCOLS DO NOT INSERT SIGNIFICANT DELAYS IN THE MESSAGE.

THE VSC RECEIVER MUST RECEIVE THE COMPLETE MESSAGE WITHIN 400 MILLISECONDS FROM THE POINT AT WHICH IT RECOGNIZES THE BEGINNING OF A MESSAGE. IF THE MESSAGE IS NOT COMPLETELY RECEIVED WITHIN THIS 400 MILLISECOND INTERVAL, THE MESSAGE PARAMETERS ARE FORCED TO FALSE. WHILE THIS IS A SAFE-SIDE FAILURE, IT MAY CREATE OPERATIONAL ISSUES IN THE MOVEMENT OF TRAINS.

4.15. EXTERNAL POWER

To provide the isolated interface a power source must be provided to power the isolated electronics of the daughter board. An on-board power supply regulates the applied voltage to five volts for the interface electronics. This power supply does not provide isolation between the external source and the daughter board electronics. When selecting a source of this external power application, the engineer should be aware that the typical data communications equipment ties the serial data signal common to earth ground. Therefore, an energy source that cannot be grounded for any reason should not be used for this power connection. Often, the data communications equipment power supply has sufficient power available to provide power to the daughter board.

4.16. TEST POINTS

Figure 4–4 shows the VSC board test point locations, while Figure 4–5 is a similar drawing of the VSC board with daughter board (T1) installed.

TP1 through TP5 and TP7 are not available on VSC boards with the daughter board (T1) installed.

Table 4–1. VSC Board Test Points

Test Points	
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP9, TP11	used in factory test
TP8	+5V, power
TP10	COM, common

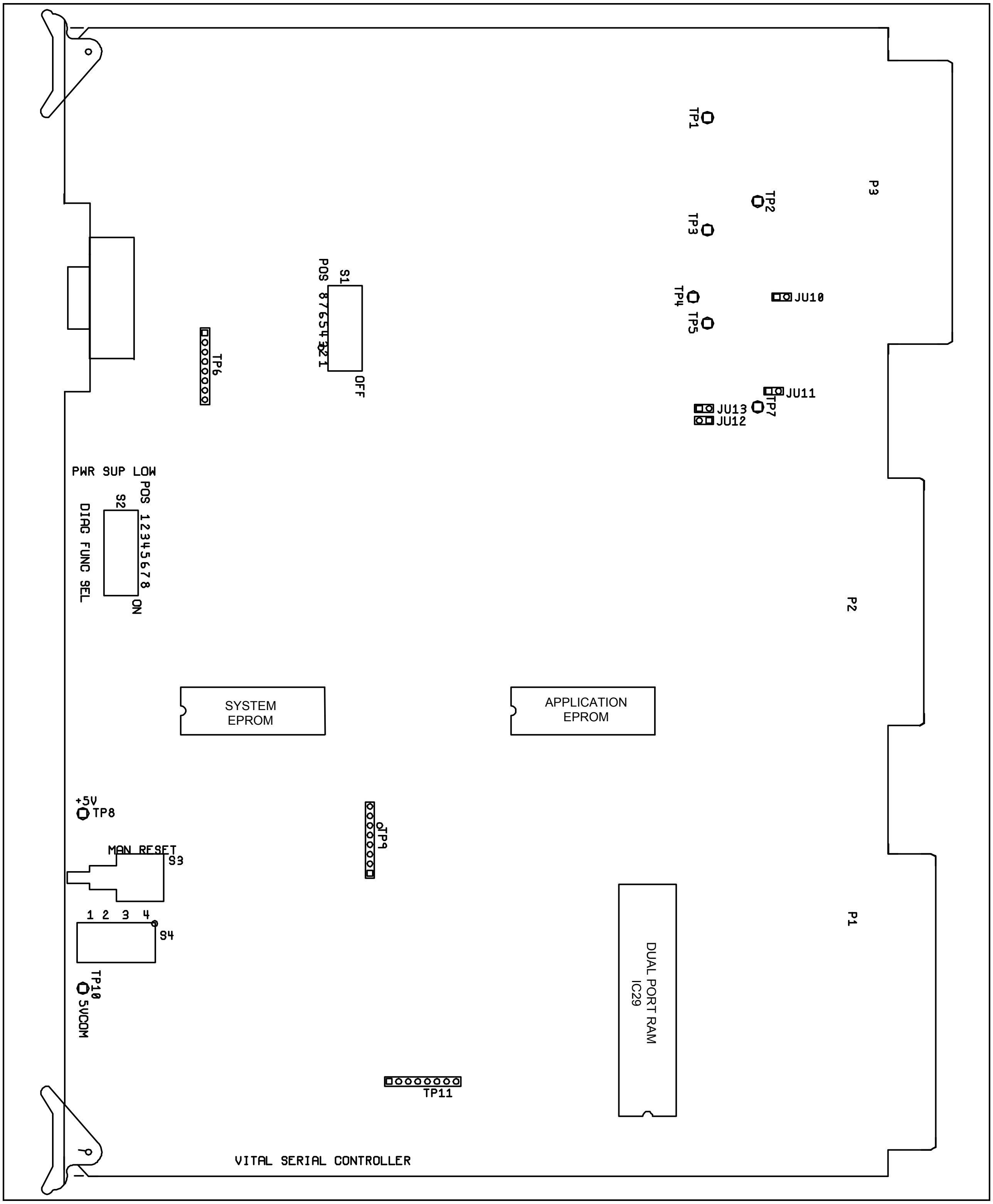

Figure 4–4. VSC Board Test Point, Switch, Jumper, and EPROM Locations

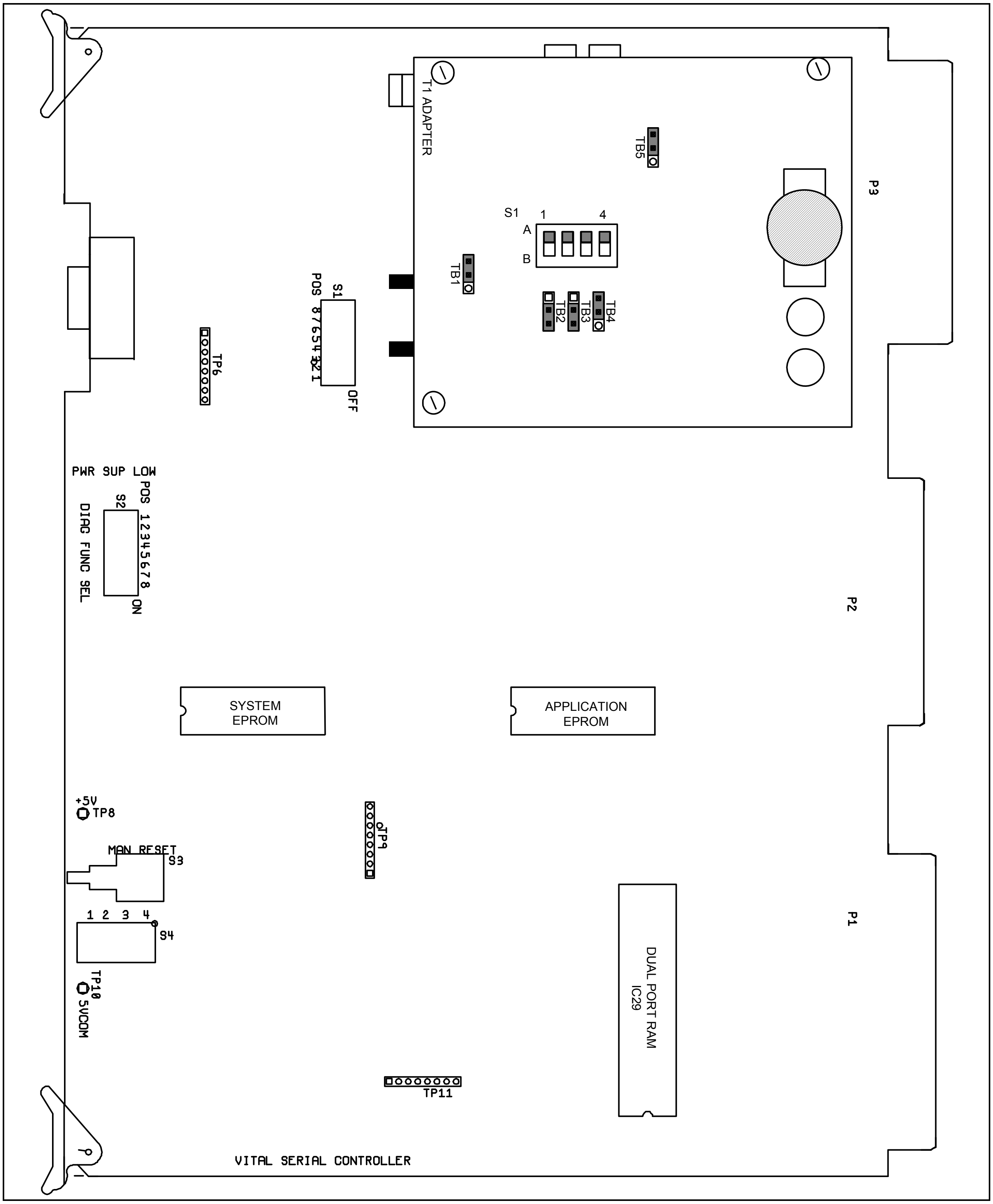

Figure 4–5. VSC Board with T1 Adapter Board Test Point, Switch, and EPROM Locations

4.17. ON-BOARD SWITCHES

There are four VSC board DIP switches, identified as S1, S2, S3, and S4. The following describes the switches and gives the function associated with each setting.

NOTE

> If a 31166-058-01 daughter board is installed, the switches S1 and S2 must be set for -11 and -18 VSC boards. If an attempt is made to operate the board through the copper wire pair interface with a daughter board installed, the board does not operate properly.

Figures 4–4 and 4–5 show the VSC board switch locations, without and with the daughter board (T1 adapter board) installed.

4.17.1. S1

S1 contains DIP switches to configure handshake signals to the SCC. Figure 4–6 lists the DIP switch 1 settings for the VSC board groups used in the VPI II system.

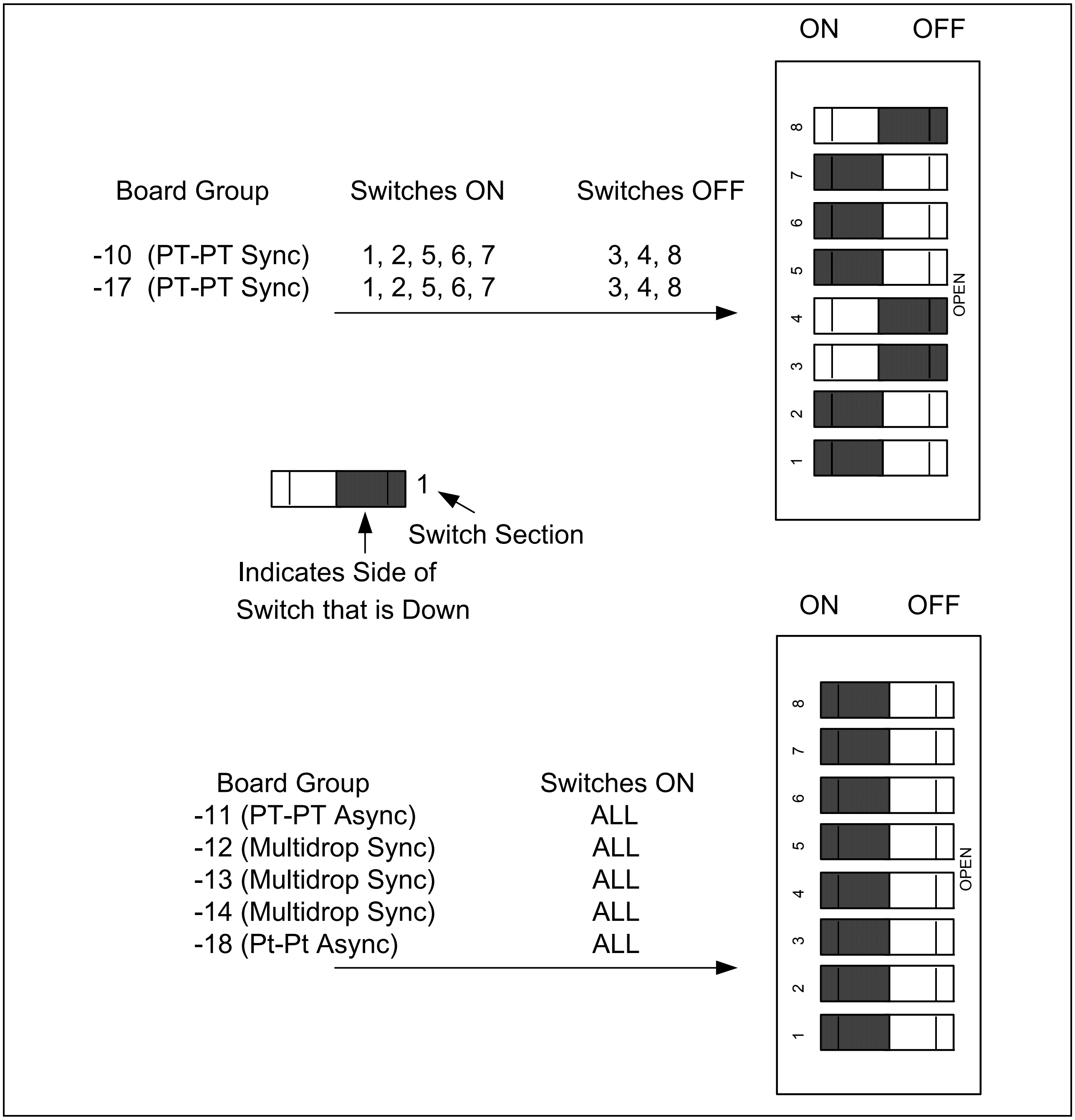

Figure 4–6. VSC Board DIP Switch S1

Table 4–2. VSC Board DIP Switch S1 Functions

Switch Position	Off	On
1	Transmit Data Out Disabled	Transmit Data Out Enabled
2	MED Transmit Sync Disabled	MED Transmit Sync Enabled
3	Non-Valid Manchester Code To SCC-CTS\ Disabled	Non-Valid Manchester Code To SCC-CTS\ Enabled
4	Not Used	Not Used
5	Receive Data From MED Disabled	Receive Data From MED Enabled
6	Transmit Clock From MED Disabled	Transmit Clock From MED Enabled
7	Receive Clock From MED Disabled	Receive Clock From MED Enabled
8	Not Used	Not Used

4.17.2. S2

This 8-position DIP switch is used for future diagnostics and operational functions. Figure 4–7 lists the DIP switch 2 settings for the VSC board groups used in the VPI II system.

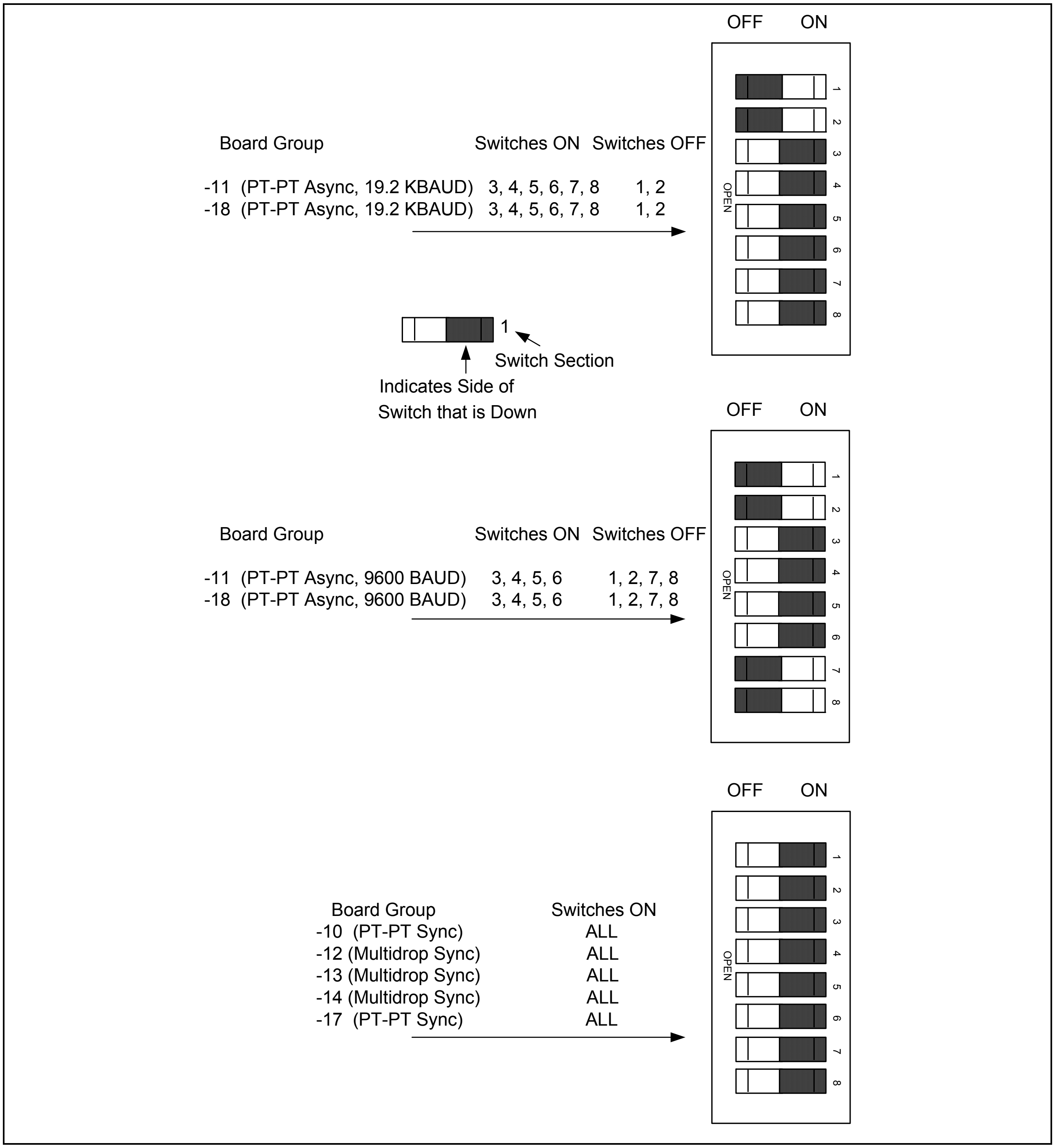

Figure 4–7. VSC Board DIP Switch S2

Table 4–3. VSC Board DIP Switch S2 Functions

Switch Position	Off	On
1	Async data 1 enabled	Sync data 1 enabled
2	Async data 2 enabled	Sync data 2 enabled
3	Not used	
4	Not used	
5	Not used	
6	Not used	
7	9600 Baud select 1	19.2 K Baud select 1
8	9600 Baud select 2	19.2 K Baud select 2

NOTE

When operating in asynchronous mode, the message format is one start bit, 8 data bits, no parity bit and two stop bits. The communication equipment selected must be able to support this format.

The BAUD rate is selectable for Async mode only.

4.17.3. S3

S3 is a VSC board reset switch.

4.17.4. S4

Memory select, reset inhibit, etc. Figure 4–8 shows the DIP switch 4 settings used for all VSC board groups used in the VPI II system.

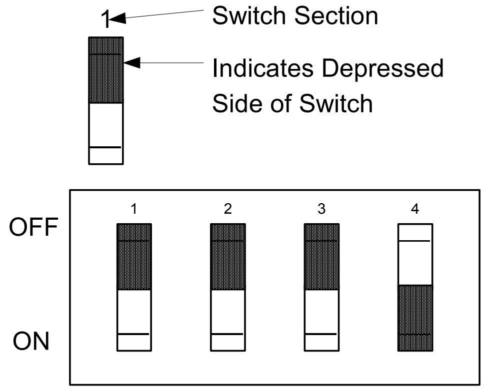

Figure 4–8. VSC Board DIP Switch S4

Table 4–4. VSC S4 Miscellaneous Functions

Switch Position	Off	On
1	Enable Auto Watchdog Reset	Disable Reset
2	Memory Select 16K X 8 EPROM (System, U16)	Memory Select 32K X 8 EPROM (System, U16)
3	Memory Select 16K X 8 EPROM (Application, U18)	Memory Select 32K X 8 EPROM (Application, U18)
4	Select Alternate Reset Vector	Select Normal Reset Vector

WARNING

ALTHOUGH THE VSC BOARD ASSEMBLY IS EQUIPPED WITH A 9-PIN CONNECTOR THAT IS SIMILAR TO THAT USED BY OTHER PROCESSORS FOR DIAGNOSTIC INFORMATION AND ACCESS TO INTERNAL STATUS, THERE ARE NO DIAGNOSTICS AVAILABLE WITH THIS BOARD ASSEMBLY. ATTEMPTS TO ACCESS DIAGNOSTICS ON THIS ASSEMBLY MAY RESULT IN INTERRUPTION TO THE OPERATION OF THE VSC FUNCTIONS AND VSC PARAMETERS. THIS IN TURN MAY AFFECT THE OPERATION OF THE INTERLOCKINGS THAT DEPEND UPON THE VSC PARAMETERS.

The following jumpers affect the operation of the direct wire interface only. When using the P/N 31166-058-01 daughter board they have no effect on the board operation. Refer to Table 4–5 and Figure 4–4 for the location of the VSC board jumpers.

Table 4–5. Line Termination Jumpers for Copper Pair Interface

Jumper	Installed	Function/Explanation
JU10	Yes	Connects the back-to-back junction of suppressors CR6 & CR7 to the logic common. This provides transient protection for the direct wire transmitter.
JU11	Yes	Connects the back-to-back junction of suppressors CR4 & CR5 to the logic common. This provides transient protection for the direct wire receiver.
JU12	No	Transmitter output level 1:2 (JU13 not installed)
JU13	Yes	Transmitter output level 1:1 (JU12 not installed)

4.18. CARD EDGE CONNECTORS

The VSC Board has three card edge connectors:

- P3, the top connector, 36-pin connector wired to the isolated serial I/O for both VPI-VPI and VPI-OTHER links
  - See Table 4–6 for 36 -pin configuration details
- P2, the middle connector, is a 50-pin connector wired to the VPI Motherboard that contains 5V power and system address programming
  - P2-42 through P2-47 are wired in a specific pattern to common on P2-48 per the application .lvc CAAPE report for board addressing; the remaining pins are not user configurable
- P1, the lower connector, is a 60-pin connector wired to the system bus; this connector is not user configurable

When applied with a plug-coupled VPI chassis, connector P3, a 36-pin discrete wire PC edge connector, is wired to a 50-way connector on the back panel of a VPI module to permit use of a VSC standard cable. VSC edge connector, name, standard cable coordinate and function are shown in Table 4–6.

WARNING

ALTHOUGH THE VSC BOARD ASSEMBLY IS EQUIPPED WITH A 9-PIN CONNECTOR THAT IS SIMILAR TO THAT USED BY OTHER PROCESSORS FOR DIAGNOSTIC INFORMATION AND ACCESS TO INTERNAL STATUS, THERE ARE NO DIAGNOSTICS AVAILABLE WITH THIS BOARD ASSEMBLY. ATTEMPTS TO ACCESS DIAGNOSTICS ON THIS ASSEMBLY MAY RESULT IN INTERRUPTION TO THE OPERATION OF THE VSC FUNCTIONS AND VSC PARAMETERS. THIS IN TURN MAY AFFECT THE OPERATION OF THE INTERLOCKINGS THAT DEPEND UPON THE VSC PARAMETERS.

WARNING

WHEN USING ASSEMBLY VERSIONS THAT INCLUDE THE DAUGHTER BOARD AN EXTERNAL POWER SOURCE MUST BE PROVIDED. THIS ENERGY SOURCE MUST NOT BE A VITAL ENERGY OR A NON-VITAL ENERGY THAT CANNOT BE CONNECTED TO EARTH GROUND. THIS IS BECAUSE THE COMMUNICATION EQUIPMENT THAT THE DAUGHTER BOARD CONNECTS TO USUALLY CONNECTS SIGNAL COMMON, FOR EXAMPLE ISOCOM, P3-36 (PLUG COUPLER H1), TO EARTH GROUND.

Table 4–6. VSC Board 36-pin P3 Connections

P3 Pin	Name	50-Way	Signal Function
1	VPITXA	C1	VPI to VPI link transmit wire A
2	VPITXB	B5	VPI to VPI link transmit wire B
3		C3	(not used)
4		D1	(not used)
5	VPIRCVA	C5	VPI To VPI link receive wire A
6	VPIRCVB	D3	VPI To VPI link receive wire B
7		D2	(not used)
8		D5	(not used)
9		E5	(not used)
10		E2	(not used)
11		E1	(not used)
12		E3	(not used)
13		A1	(not used)
14		E4	(not used)
15		D4	(not used)
16		F1	(not used)
17		C2	(not used)
18		F2	(not used)
19		A4	(not used)
20		F3	(not used)
21	ALT.SERIAL1	B2	VPI to other XMIT/RCV LINK WIRE1
22	ALT.SERIAL2	F4	VPI to other XMIT/RCV LINK WIRE 2
23		C4	(not used)
24		F5	(not used)
25	INTERFACE OPT 1	A2	TXD *
26	INTERFACE OPT 2	G1	RTS *
27	INTERFACE OPT 3	A3	DTR *

* Indicates EIA232 signals from daughter board interface assembly -11 or -18 VSC board. Note: RTS, DTR, CTS, CD and DSR signals are not supported by the VSC system software. These signals should not be wired to any external equipment.

Table 4–6. VSC Board 36-pin P3 Connections (Cont.)

P3 Pin	Name	50-Way	Signal Function
28	INTERFACE OPT 4	G2	RXD *
29	INTERFACE OPT 5	A5	CTS *
30	INTERFACE OPT 6	G3	CD *
31	INTERFACE OPT 7	B1	DSR *
32		G4	(not used)
33		B3	(not used)
34		G5	(not used)
35	INTERFACE OPT 8	B4	IVCC (9-35VDC) *
36	INTERFACE OPT 9	H1	ISOCOM (Isolated Signal Common) *

* Indicates EIA232 signals from daughter board interface assembly -11 or -18 VSC board. Note: RTS, DTR, CTS, CD and DSR signals are not supported by the VSC system software. These signals should not be wired to any external equipment.

4.19. BOARD ASSEMBLY DIFFERENCES

The five versions of the VSC board that can be used with the VPI II system are summarized in Table 4–7. All assemblies have a maximum board logic current supply value of 500 mA.

Table 4–7. VSC Board Specifications

Ass'y No.	Type	Maximum # of Boards Per VPI System	Board Slots Required	Baud Rate	System Software
10	Pt - Pt	10 (NOTE 1)	1	19200 (Sync.)	40025-322-00 VSC
11	Pt.-Pt. with daughter board	10 (NOTE 1)	2	9600 or 19200 (Async.)	40025-322-00 VSC
12	Multi-drop full duplex 4-wire	2 (NOTE 2)	1	19200 (Sync.)	40025-323-00 MVSC (NOTE 3)
13	Multi-drop half duplex 2-wire	2 (NOTE 2)	1	19200 (Sync.)	40025-324-00 GVSC (NOTE 3)
14	Multi-drop half duplex 2-wire	2 (NOTE 2)	1	19200 (Sync.)	40025-348-00 GVSCE (NOTE 4)
17	Pt - Pt	10 (NOTE 1)	1	19200 (Sync.)	40025-406-00 VSC
18	Pt.-Pt. with daughter board	10 (NOTE 1)	2	9600 or 19200 (Async.)	40025-406-00 VSC

NOTE 1: This limit is 10 minus the sum of (#VSC + #MVSC + #GVSC + #GVSCE + #CRG + #CSEX), where # indicates the total number of a particular VPI board type.
NOTE 2: The total number of GVSCE + GVSC + MVSC combinations must be less than or equal to 2.
NOTE 3: Supports 15 parameters per track.
NOTE 4: Supports 25 parameters per track.

4.20. VSC DAUGHTER BOARD, P/N 31166-058-XX

Figure 4–9 provides a graph of Daughter board current versus voltage, while Figure 4–10 shows the board layout.

WARNING

WHEN USING ASSEMBLY VERSIONS THAT INCLUDE THE DAUGHTER BOARD AN EXTERNAL POWER SOURCE MUST BE PROVIDED. THIS ENERGY SOURCE MUST NOT BE A VITAL ENERGY OR A NON-VITAL ENERGY THAT CANNOT BE CONNECTED TO EARTH GROUND. THIS IS BECAUSE THE COMMUNICATION EQUIPMENT THAT THE DAUGHTER BOARD CONNECTS TO USUALLY CONNECTS SIGNAL COMMON, FOR EXAMPLE ISOCOM, P3-36 (PLUG COUPLER H1), TO EARTH GROUND.

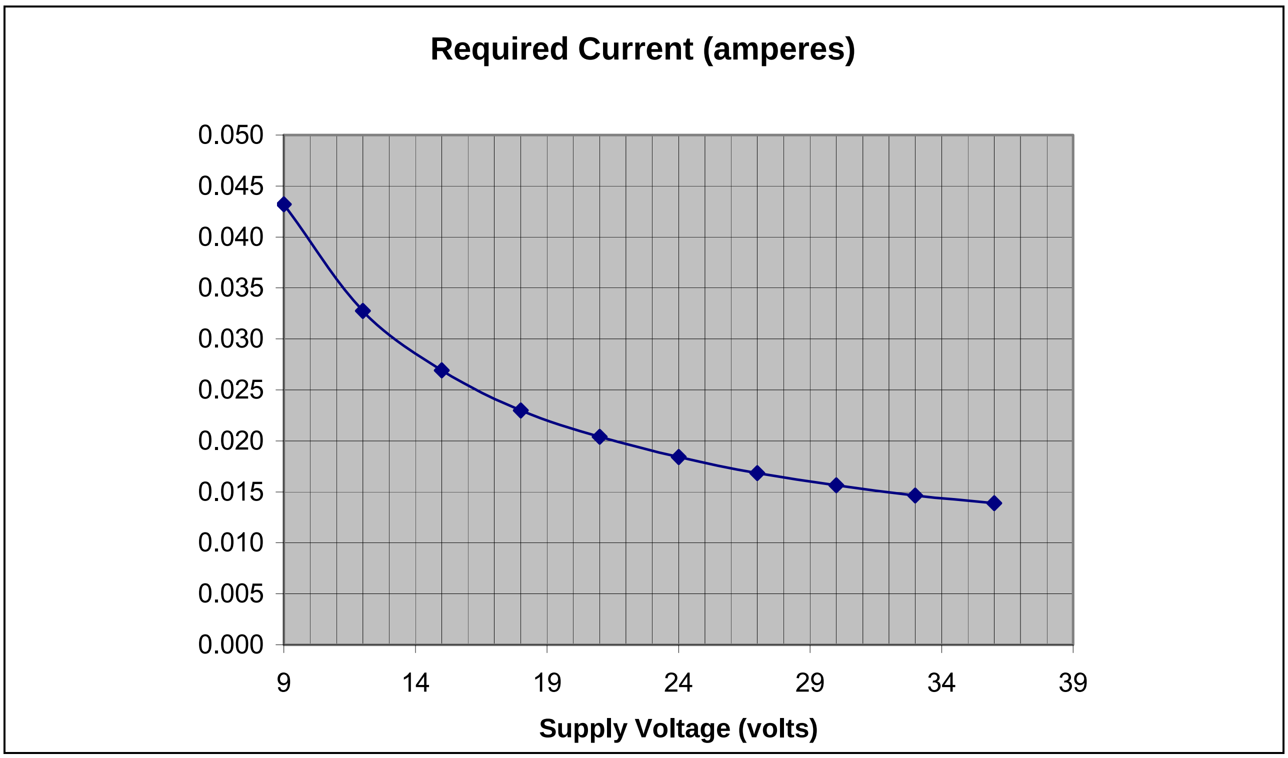

Figure 4–9. Daughter Board Current vs. Voltage

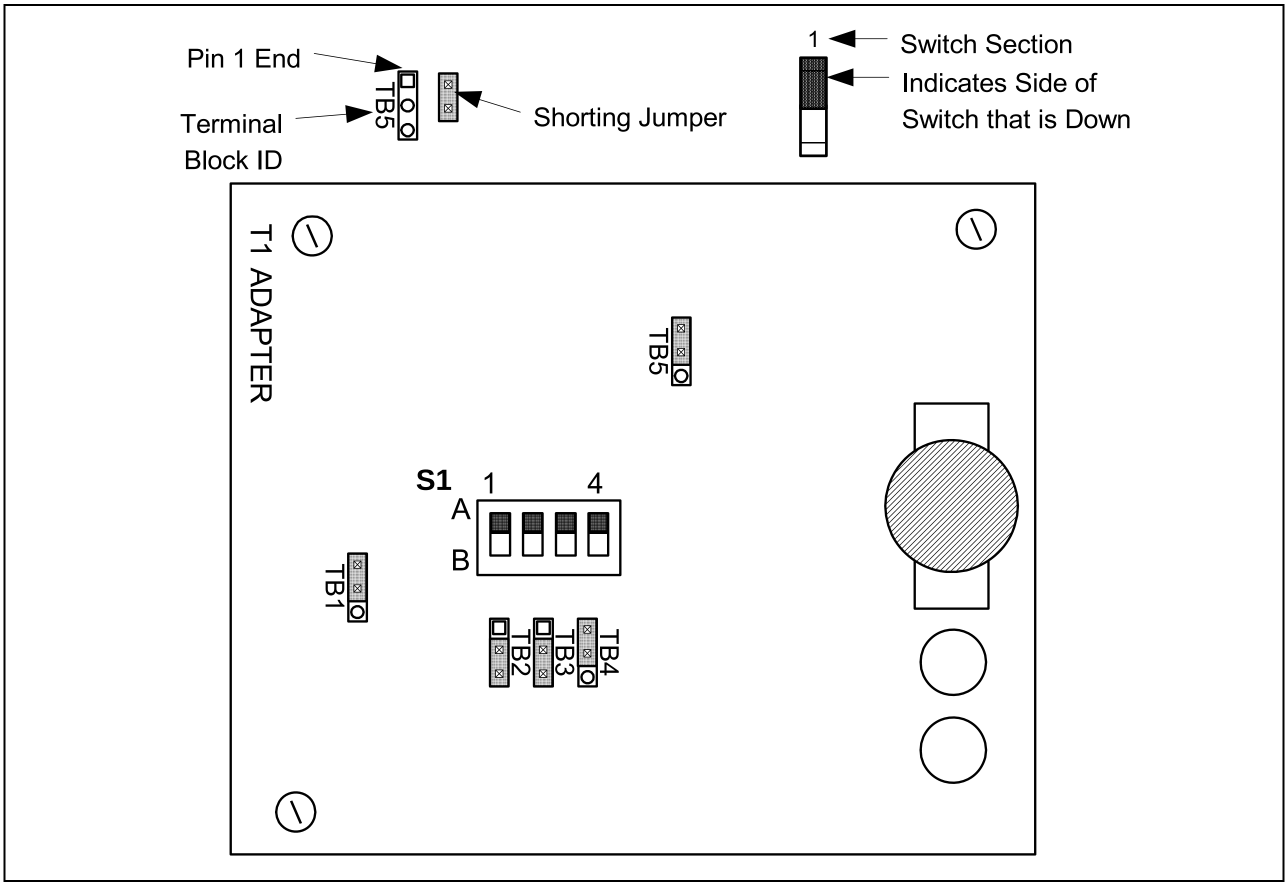

Figure 4–10. VSC Daughter Board

For normal operation of the daughter board, all sections of S1 should be set in the “A” position. There are five (5) terminal blocks on the daughter board. These terminal blocks support special manufacturing and development functions and should not be altered in applying this assembly.

For their operating positions, refer to Table 4–8.

Table 4–8. Daughter Board Terminal Block Operating Positions

Terminal Block	Jumper Position
TB1	1-2
TB2	2-3
TB3	2-3
TB4	1-2
TB5	1-2

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5. SECTION 5 – CRG (CODE RATE GENERATOR) BOARD, P/N 31166-261-XX

5.1. INTRODUCTION

This section provides CRG board detail.

5.2. GENERAL

The Code Rate Generator (CRG) board is a Vital VPI board that receives Vital commands from the CPU II board, generates codes outputs based on the commands, and transmits non-vital output status back to the CPU II board.

5.3. OPERATION

The CRG board receives code rate commands from the VPI CPU II board. The received code rate commands are decoded and used to generate 8 coded outputs. The frequency and duty-cycle of the coded outputs are vitally verified by using an Absence Of Current Detector (AOCD). Data is circulated through the AOCD. Data returned from the AOCD coupled with other NISAL processing verifications are used to generate a message that the CRG board sends to the VPI CPU II board. The message received by the CPU II board from the CRG is used as part of the generation of the VRD checkwords. All outputs are generated using a Double Break Output (DBO) DC-DC converter and as such, are isolated from each other by >2000Vrms and protected from undetected single-fault failures. A system block diagram is shown in Figure 5–1.

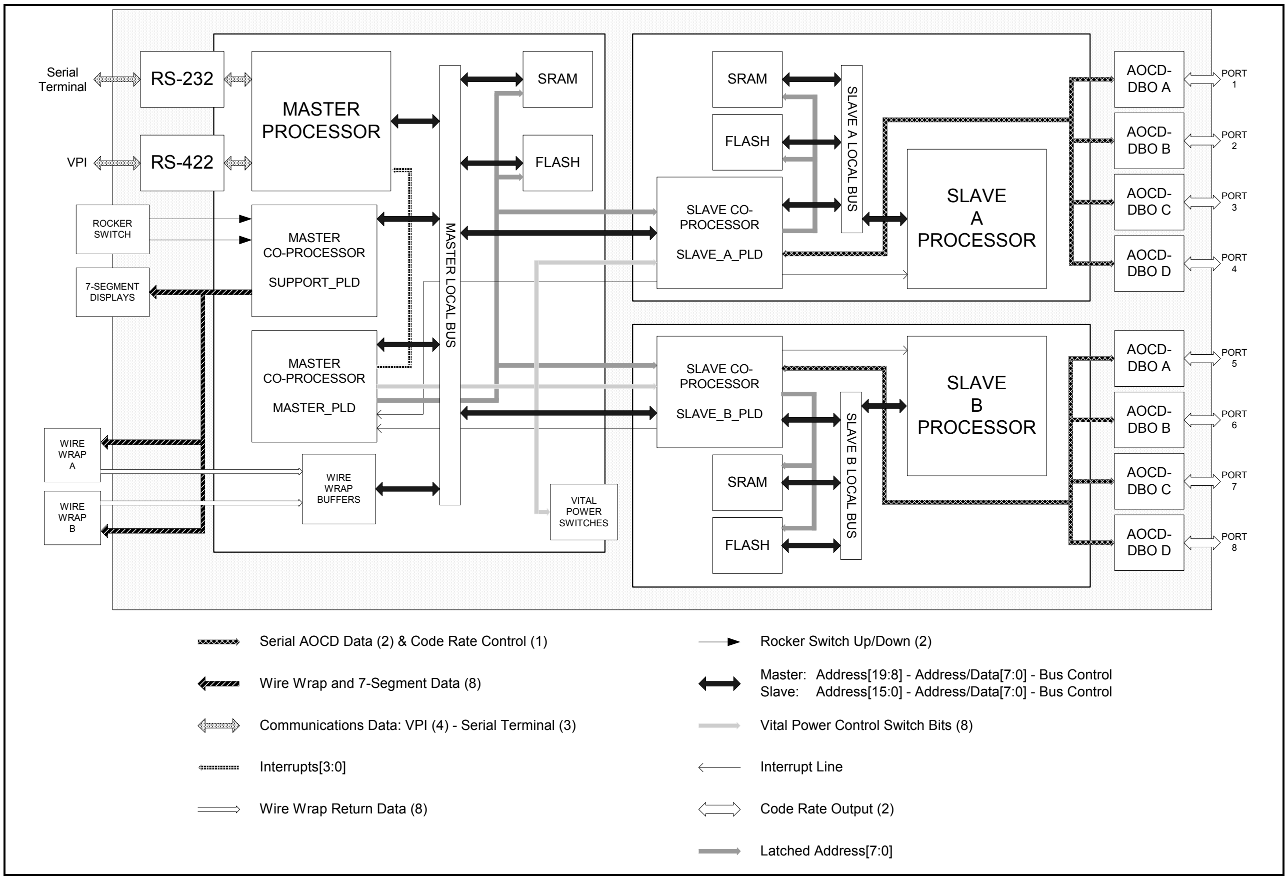

Figure 5–1. CRG Board Block Diagram

5.4. INDICATIONS

The CRG board has two displays, a rocker switch, and a reset switch, as shown in Figure 5–2.

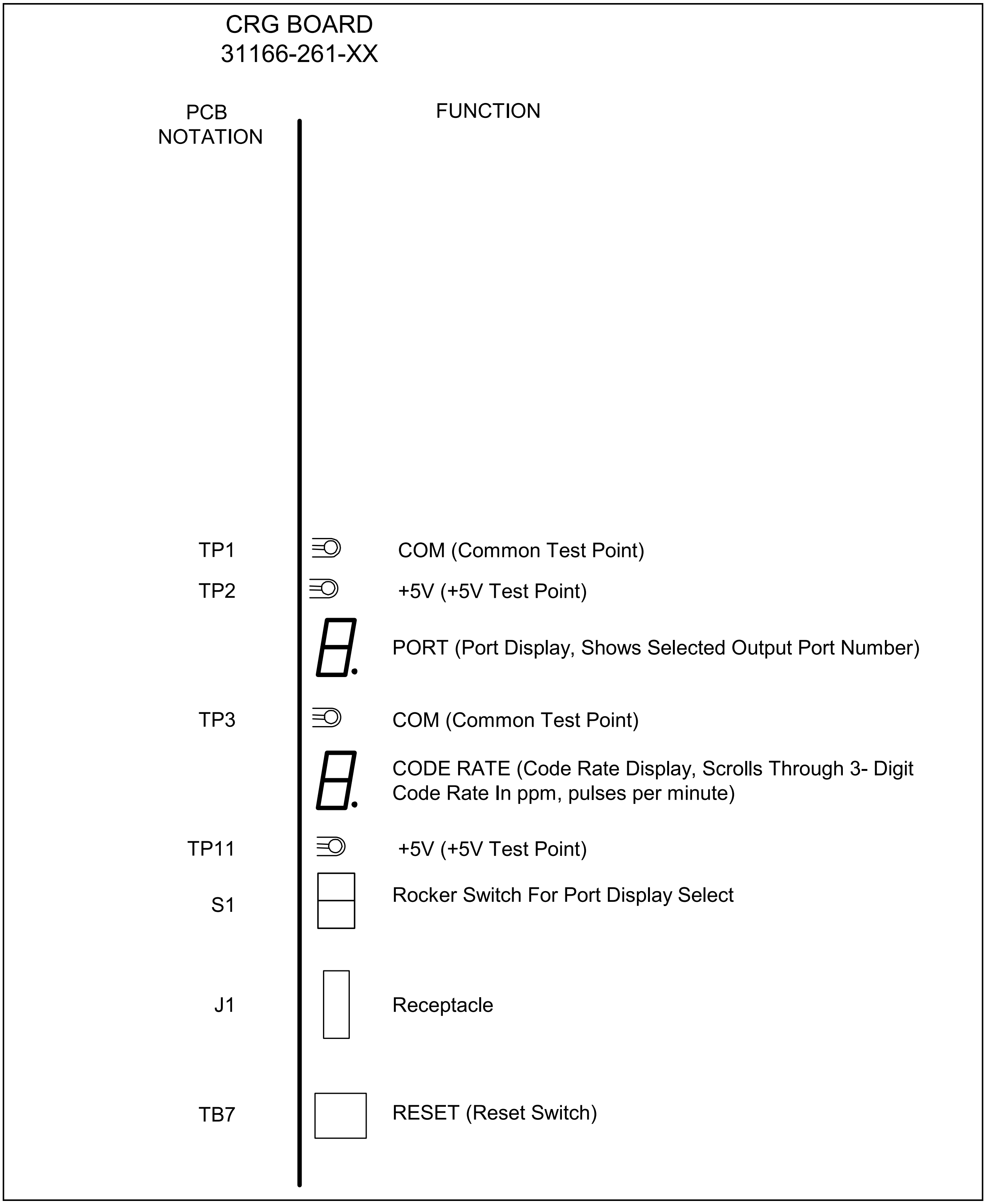

Figure 5–2. CRG Board Edge

5.5. ELECTRICAL RATINGS

The +5V power supply has a voltage range of 4.75V to 5.25V and typical operating current of 1.15A.

The +12V power supply (VRD energy) has a voltage range of 8V to 16V and a typical operating current on 0.5A.

5.6. OUTPUTS

The code rate outputs are sent through the P3 connector from a Solid State Driver or a B-Relay Driver.

5.6.1. Solid State Relay Driver

The output circuit on a solid state driver is designed to drive a CRYDOM D241xx type Solid State Relay. Because the relay itself is non-vital, with an operating current in the range of the Vital detection threshold of the AOCD (3mA), a parallel, wire-wound, established reliability resistor, mounted in a four-terminal configuration, is used to guarantee a minimum current draw of 4mA at the minimum turn-off voltage of the CRYDOM relay (1V).

Nominal Operating Conditions (load 1500Ω):

- Output Voltage: ~4.64V
- Output Current: ~3.1mA

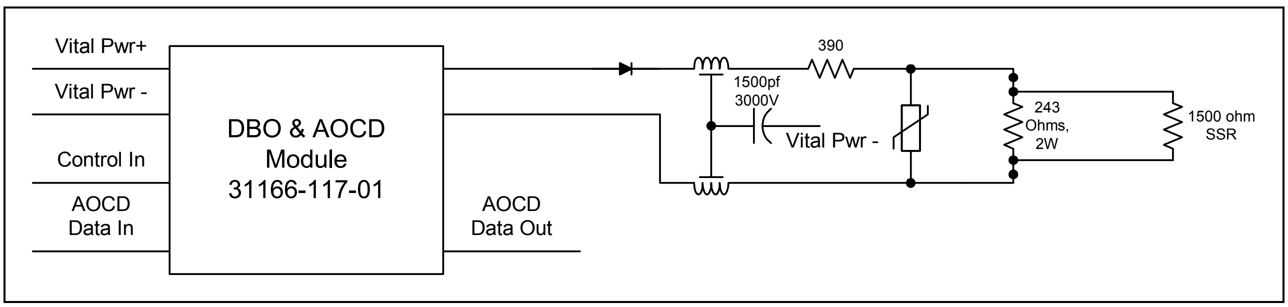

Figure 5–3. Output Circuit Solid State Relay Driver

The values listed below are calculated considering worst case conditions. Component values and power supply voltages are chosen to yield a result at the extreme of the condition in question.

Load Short-Circuit:

- Max Current (16V into DBO-AOCD): ~50mA
- Min Current (8V into DBO-AOCD): ~24mA

Load Open-Circuit:

- Max Voltage (16V into DBO-AOCD): ~7.38V
- Min Voltage (8V into DBO-AOCD): ~3.29V

5.6.2. B-Relay Driver

The output circuit on a relay driver is designed to drive a typical B-style code following relay. The equations listed below allow for the computation of the output voltage and current as function of Vital power supply voltage and relay coil impedance.

Nominal Operating Conditions (VS = Vital Power Supply Voltage; RL = Coil Impedance):

- Output Voltage: VOUT = VS*(1.2) - (~0.7)
- Output Current: IOUT = VOUT/RL

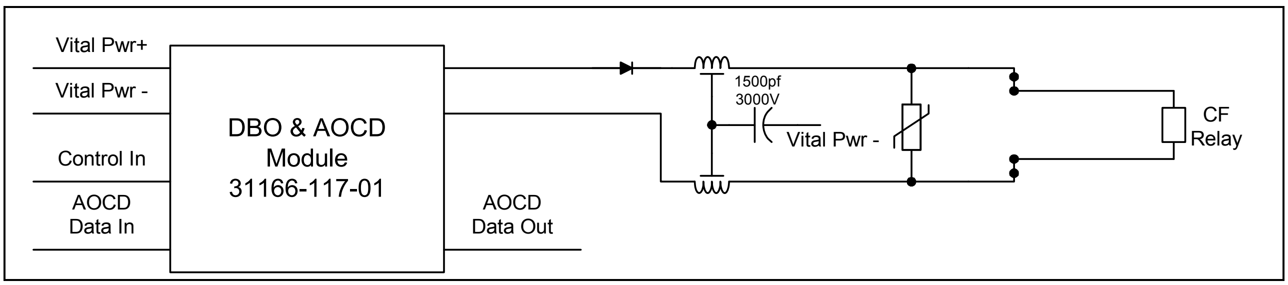

Figure 5–4. Output Circuit B-Relay Driver

5.7. COMMUNICATIONS

Table 5–1. CRG Board Communications Specifications

Specification	Serial Port 1 (EIA232)	Serial Port 0 (EIA422)
Mode of Operation	Single-ended	Differential
Total Number of Drivers and Receivers on 1 Line	1 Driver 1 Receiver	1 Driver 10 Receivers
Maximum Cable Length	50 ft.	4000 ft.
Maximum Data Rate	20kb/s	10Mb/s
Maximum Driver Output Voltage	± 25V	-0.25V to +6V
Driver Output Signal Level (loaded minimum)	5V to 15V	± 2V
Driver Output Signal Level (unloaded maximum)	± 25V	± 6V
Driver Load Impedance	3kΩ to 7kΩ	100Ω
Maximum Driver Current in High Z State (power off)	± 6mA @ ± 2V	± 100цA
Maximum Slew Rate	30.0V/цs	N/A
Receiver Input Voltage Range	± 15V	-10V to +10V
Receiver Input Sensitivity	± 3V	± 200mV
Receiver Input Impedance	3kΩ to 7kΩ	4kΩ min.

5.8. TEST POINTS

Figure 5–5 shows the CRG board test points and switches.

Table 5–2. CRG Board Test Points

Test Points	
TP1, TP9	COM, common
TP2, TP11	+5V, power
TP3, TP4, TP5, TP6, TP7, TP8, TP10, TP12 through TP38	used in factory test

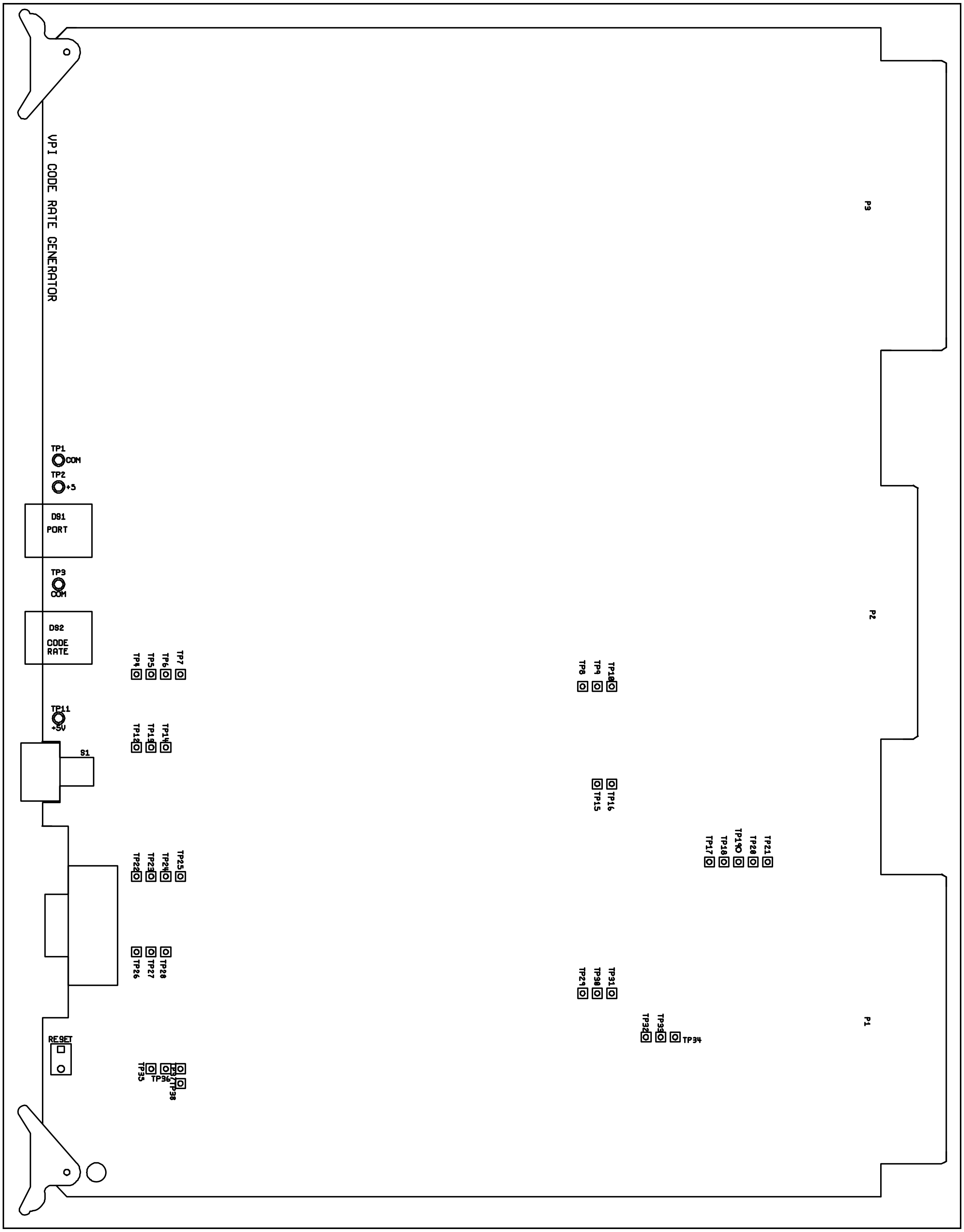

Figure 5–5. CRG Board Test Point and Switch Locations

5.9. CARD EDGE CONNECTORS

The CRG board has three card edge connectors:

- P3, the top connector, is a 36-pin connector which contains wiring for code rates 1 through 8 and Vital power connections
  - See Table 5–3 for 36-pin configuration details
- P2, the middle connector, is a 50-pin connector used for connections to the motherboard which supplies 5 Volt power and common; this connector is not user configurable
- P1, the lower connector, is a 36-pin connector which contains wiring for check ids and serial links
  - See Table 5–4 for 36-pin configuration details
  - The ID pins on P1 are wired in a specific pattern per the application .lvc CAAPE report for board addressing

Table 5–3. CRG Board 36-pin P3 Connections

P3-	Name	Function
1	CODE_RATE_8-	Code Rate 8
2	CODE_RATE_8+	Code Rate 8
3		(not used)
4		(not used)
5	CODE_RATE_7-	Code Rate 7
6	CODE_RATE_7+	Code Rate 7
7		(not used)
8		(not used)
9	CODE_RATE_6-	Code Rate 6
10	CODE_RATE_6+	Code Rate 6
11		(not used)
12		(not used)
13	CODE_RATE_5-	Code Rate 5
14	CODE_RATE_5+	Code Rate 5
15		(not used)
16		(not used)
17	CODE_RATE_4-	Code Rate 4
18	CODE_RATE_4+	Code Rate 4
19		(not used)
20		(not used)
21	CODE_RATE_3-	Code Rate 3
22	CODE_RATE_3+	Code Rate 3
23		(not used)
24		(not used)
25	CODE_RATE_2-	Code Rate 2
26	CODE_RATE_2+	Code Rate 2
27		(not used)
28		(not used)
29	CODE_RATE_1-	Code Rate 1
30	CODE_RATE_1+	Code Rate 1

Table 5–3. CRG Board 36-pin P3 Connections (Cont.)

P3-	Name	Function
31		(not used)
32		(not used)
33	VPC+	Vital Power +
34	VITAL_POWER-	Vital Power Common
35	VPC+	Vital Power +
36	VITAL_POWER-	Vital Power Common

Table 5–4. CRG Board 36-pin P1 Connections

P1-	Name	Function
1	GEN_OUT_A0	Generated Output A0
2	GEN_OUT_A1	Generated Output A1
3	GEN_OUT_A2	Generated Output A2
4	GEN_OUT_A3	Generated Output A3
5	GEN_OUT_A4	Generated Output A4
6	GEN_OUT_A5	Generated Output A5
7	GEN_OUT_A6	Generated Output A6
8	GEN_OUT_A7	Generated Output A7
9	CHECK_ID2_0	ID Check 2_0
10	CHECK_ID2_1	ID Check 2_1
11	CHECK_ID2_2	ID Check 2_2
12	CHECK_ID2_3	ID Check 2_3
13	CHECK_ID2_4	ID Check 2_4
14	CHECK_ID2_5	ID Check 2_5
15	CHECK_ID2_6	ID Check 2_6
16	CHECK_ID2_7	ID Check 2_7
17	CHECK_ID1_0	ID Check 1_0
18	CHECK_ID1_1	ID Check 1_1
19	CHECK_ID1_2	ID Check 1_2
20	CHECK_ID1_3	ID Check 1_3
21	CHECK_ID1_4	ID Check 1_4
22	CHECK_ID1_5	ID Check 1_5
23	CHECK_ID1_6	ID Check 1_6
24	CHECK_ID1_7	ID Check 1_7
29	CRG_VPI-	CRG to VPI -
30	CRG_VPI-	CRG to VPI -
31	CRG_VPI+	CRG to VPI +
32	CRG_VPI+	CRG to VPI +
33	VPI_CRG-	VPI to CRG -

Table 5–4. CRG Board 36-pin P1 Connections (Cont.)

P1-	Name	Function
34	VPI_CRG-	VPI to CRG -
35	VPI_CRG+	VPI to CRG +
36	VPI_CRG+	VPI to CRG +

5.10. BOARD ASSEMBLY DIFFERENCES

The maximum board logic current supply for all versions is 1200 mA.

Table 5–5. CRG Board Assembly Differences

Ass'y No.	Output Driver	Maximum # of Boards per VPI System	Board Slots Required	Program Numbers	Code Rates Supported (Pulses Per Minute)
03	Solid State	3	1	40025-235	0, 50, 75, 120, 180 (Parameters 6-10 are not used)
04	B-Relay	3	1	40025-325	0, 50, 75, 120, 180, 270, 420, Steady On (Parameters 9-10 are not used)

See Table A– 1 located in Appendix A (CRG Application Guidelines) of Alstom Publication P5011B, Volume 5 for rate parameter assignment details.

5.11. BOARD ASSEMBLY CODE RATES – RATE TOLERANCE

The tolerance data summarized in Table 5–6 is required when applying the CRG board.

Table 5–6. CRG Board Assembly Code Rate Tolerances

Nominal PPM	Actual PPM	On-Time msec	Off-Time msec
50	50.0	600	600
75	75.0	400	400
120	120.0	250	250
180	181.8	165	165
270	272.7	110	110
420	428.6	70	70

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6. SECTION 6 – IOB (I/O BUS INTERFACE) BOARD, P/N 59473-827-XX

6.1. INTRODUCTION

This section provides IOB board detail.

6.2. GENERAL

The I/O Bus Interface (IOB) board serves as a buffer between the system processing boards and Vital I/O. It provides a storage medium for test data obtained during Vital input and output port checks. The board includes logic to control the continuous verification of Vital output port states.

6.3. OPERATION

Figure 6–1 shows the IOB interface block diagram.

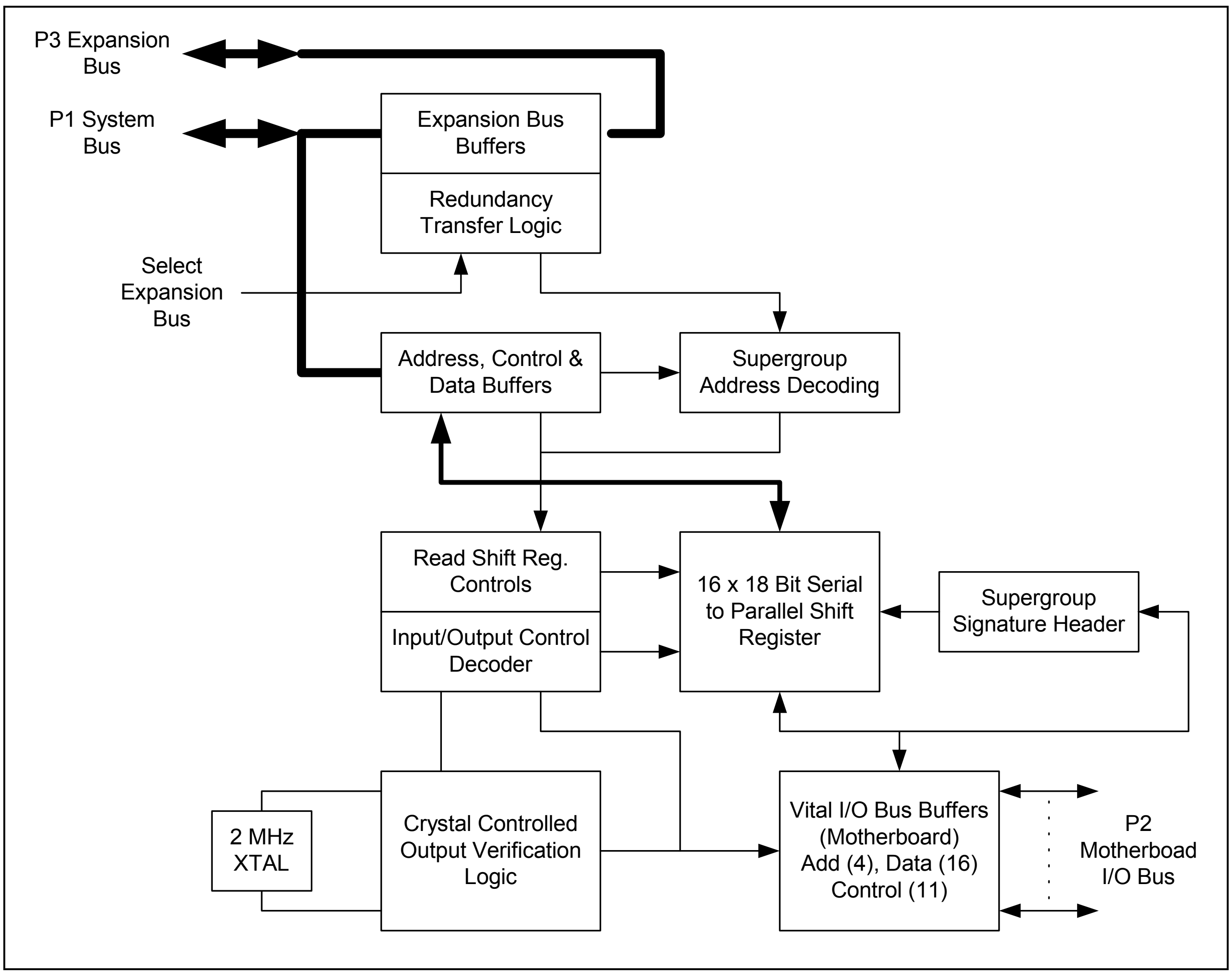

Figure 6–1. IOB Board Block Diagram

Address, control and data signals are buffered for use within the IOBUS logic. While address and control buffers are always enabled, the data buffers are only active when the IOBUS is specifically addressed.

A 7-bit address decoder compares a system bus address with that programmed for the slot in which the interface board resides (slot address inputs are labeled ADD SEL 0, 1, 2, 3). A particular bus interface board and its associated I/O are referred to as a supergroup. If bus and slot address agree, the SUPERGROUP SELECTED signal enables the data buffers. If the bus address for Vital I/O is greater than that programmed for the system module interface board, then the EN EXP DBUS control signal is generated to allow data to be obtained from expansion I/O modules in multi-module configurations.

The IOBUS logic provides buffering for links between the main system module and all expansion modules via five octal buffers and a 60-way cable. Actual data transfers occur only when the external data bus is enabled from the main system module, by jumpering P2-35 to P2-48 on the IOBUS board. The EN EXP DBUS signal is permanently disabled for interface boards in expansion modules by inserting a jumper between the proper pins on the Motherboard. The system module expansion bus can drive several expansion I/O modules.

Expansion bus buffer logic supports usage of redundant systems; that is, two sets of system electronics in a system module and Vital I/O in expansion modules. An optically-isolated input (SEL EXP BUS), derived from redundancy transfer logic, activates either of the two sets of redundant system electronics, with each having an I/O bus interface board. A 24V signal at SEL EXP BUS allows one of the two sets of system redundant electronics to communicate with the expansion I/O bus via the buffered expansion bus. When the SEL EXP BUS signal is removed, signaling a system failure, the SEL EXP BUS input is energized on the spare interface board to allow the backup set of system electronics to communicate to the Vital I/O. Vital input and output functions are controlled through memory-mapped address operations. An input/output control decoder employs three address bits to perform four tasks. The first control (YIN) represents a signal that is later gated with a read or write control when operations involving Vital inputs are performed.

The second control (YADR-YSR), when gated with a write control, sets the I/O group address latch. It is also gated with a read control to enable the reading of the bank of 16 shift registers.

The third control (YOF) signifies a write operation to Vital output boards (output state control latches), while the fourth control (YSM) is used to clock the mode latch used in output state verification.

The Vital I/O group address latch is buffered and is used to address each Vital I/O slot on the Motherboard (I/O bus) bus.

6.4. VITAL CONTINUOUS OUTPUT VERIFICATION (50 MS RECHECK CYCLE)

Output state verification is performed by a crystal controlled logic sequence and a mode latch. Data representing a desired function are loaded into the mode latch with the YSM signal. The mode latch performs one of five functions:

1. Selects mode of output verification (recheck)
2. Initiates selected mode
3. Clears logic for subsequent operations
4. Enables the highest 8 sequence/counter stages
5. Selects between an even or an odd recheck cycle

The board contains a 2-MHz crystal that drives a 14-stage counter. Function timing is controlled using specific counter stages. One output, a 125 kHz signal, is used for data modulation and another is used for the output recheck clock. Outputs of the mode latch, gated with different counter outputs, perform these functions:

- Read mode 1: the data in output board RAM is read into the shift registers (SR LOAD) as 8 serial bits, 16 bits wide and processed four times to obtain the 32-bit check data word for each output.
- Write mode 2: fills all RAM on the output boards with logic ones as an initialization process. Control signal CLR CNTR is generated in this mode while the recheck clock is disabled.
- Circulate mode 3: the circulate mode occurs 45 out of every 50 ms. The recheck clock is provided during this time to all output boards causing output port check data to be circulated and stored. Control signals C1 and C2 control this operation for even and odd recheck cycles.
- Circulate mode 4: this is the same as circulate mode 3 except that the circulation process is interrupted after 1 ms. At this time the output state may be changed to enforce special output checks, for example, hot and cold filament checks.

The 16-bit I/O data bus forwards data derived from input port tests, output port tests and Vital timer operation to a serial input of each register, which is shifted in 8-bit blocks. The registers are then accessed by the main CPU where the data is retrieved in parallel format.

Each register's serial input is dedicated to an I/O data bus line. This allows the system to access 16 Vital inputs or Vital outputs. Data is loaded into the register either by a read operation (INTMRD) with YIN active or by the output verification logic. The registers are accessed by a memory read operation with YADR-YSR active. A 3-to-8 decoder provides a register pair output enable signal based on the state of three address bits, when registers are read by the CPU.

Data derived from outputs is connected directly to the register shift left input. Input test data, however, is obtained from the I/O bus and routed through a SIGNATURE header. This header possesses 16 input-to-output path assignments, the output of which is connected to each of the 16 register shift right inputs. Each header takes as an input a certain data bus line and swaps it with another. For example, header input is data bus 1 and output is routed to data bus 9, which is tied to shift register 9. This scrambling of the data bus when reading Vital input data is used to verify correct Vital input addressing.

IOBUS logic controls the Vital I/O bus that communicates over the system Motherboard. It provides buffered outputs for board addressing (IOAB1-4), data passage via bi-directional data bus (IODB0-F), read and write data controls, output recheck controls, and memory mapped controls for communicating with a Vital timer (T-OUTC3, TIMC4). T-OUTC3 also accesses the low current output check circuitry on a lamp drive output board.

6.5. INDICATORS

The two IOB board LED indicators are shown in Figure 6–2.

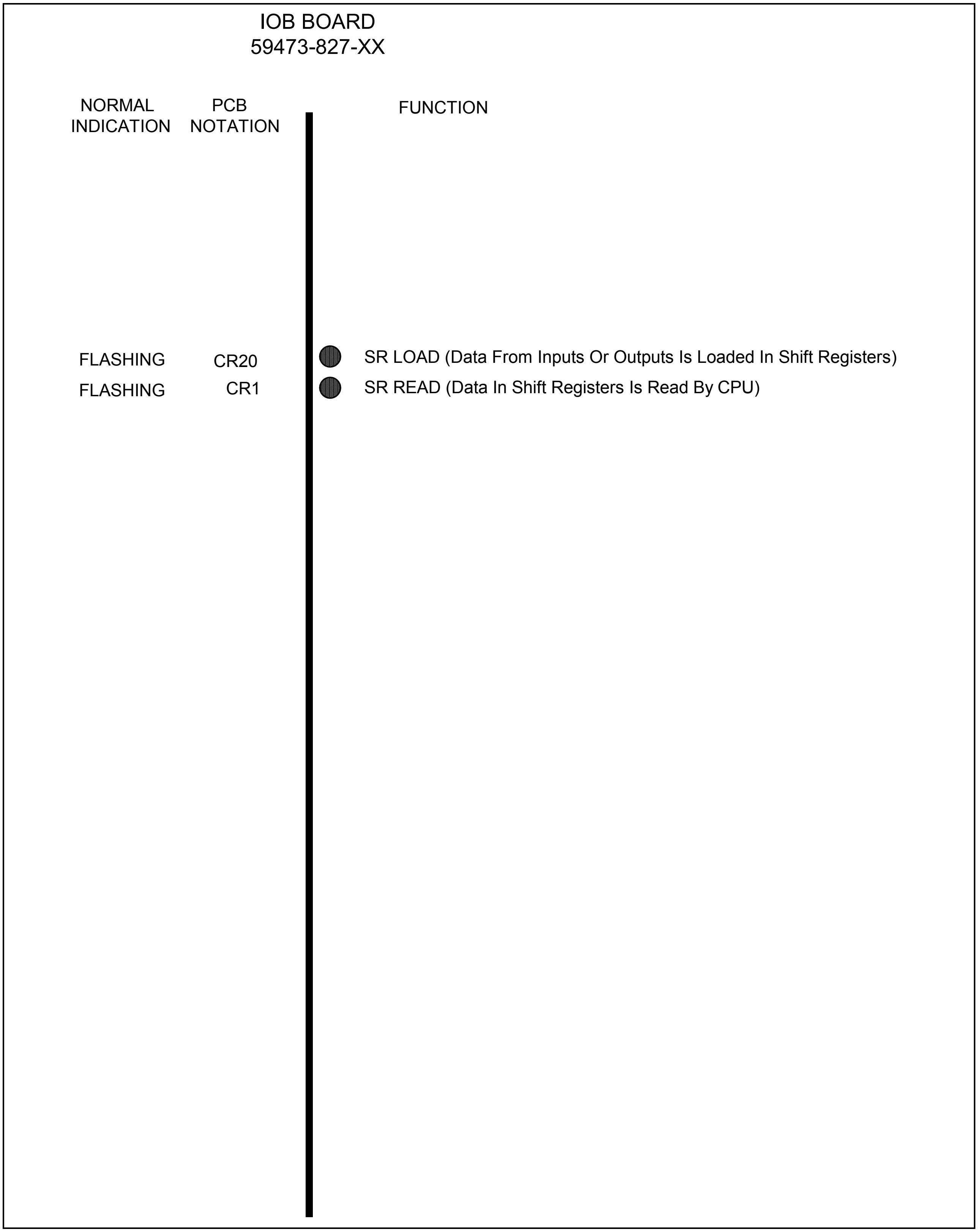

Figure 6–2. IOB Board Edge

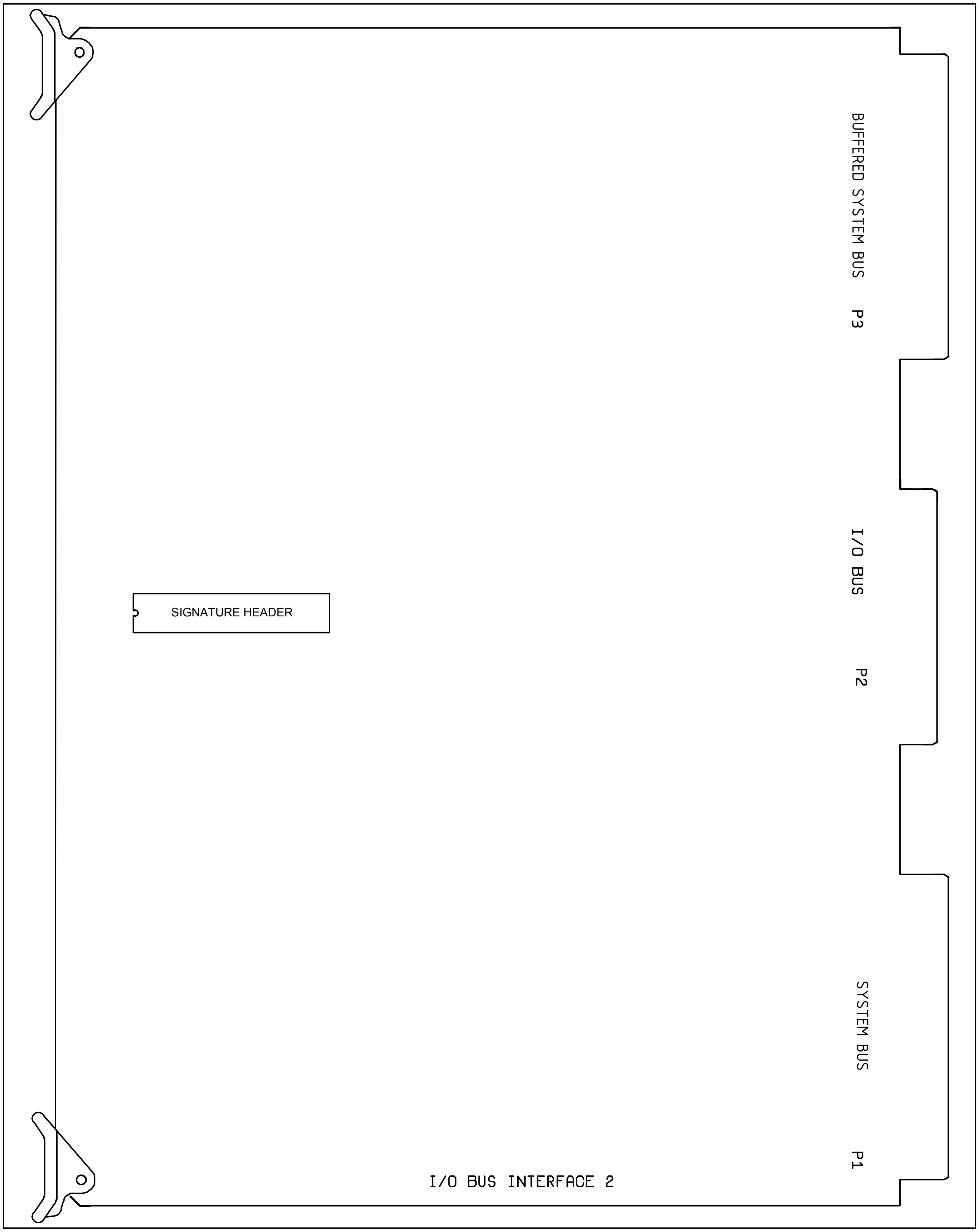

Figure 6–3. IOB Board Interface Connections and Signature Header Locations

6.6. CARD EDGE CONNECTORS

The IOB Board has three card edge connectors.

- P3, the top connector, is a 60 pin connector containing the buffered main bus used to drive expansion I/O modules
- P2, the middle connector, is a 50-pin connector that carries board power and address selection signals; connects to the motherboard which supplies 5 Volt power and common
  - P2-35 and P2-44 through P2-47 are wired in a specific pattern to common P2-48 per the application .lvc CAAPE report for board addressing; the remaining P2 pins are not user configurable
- P1, the lower connector, is a 60-pin connector containing the main address, data, and control bus for the VPI system

NOTE

The expansion bus is used in applications where more than one module is required to handle Vital or Non Vital I/O. It interfaces to either an I/O Interface Bus Board, VSC Board, or a CSEX board

6.7. SPECIFICATIONS

Table 6–1. IOB Board Bus Interface Specifications

Specification	59473-827-01
Maximum Number of Boards Per VPI System	4
Board Slots Required	1
Maximum Board Logic Current Supply	300 mA
Signature Header 59473-871-01	Board 1
Signature Header 59473-871-02	Board 2
Signature Header 59473-871-03	Board 3
Signature Header 59473-871-04	Board 4

7. SECTION 7 – DI (DIRECT INPUT) BOARD, P/N 59473-867-XX

7.1. INTRODUCTION

This section provides DI board detail.

7.2. GENERAL

Direct Input (DI) boards contain 16 isolated Vital inputs, each requiring two connections to the field (-IN and +IN). The inputs are DC current sensing and require a minimum of 12.8 mA. The maximum input current is 33 mA. Two inputs may be connected in parallel with opposite polarity (input A+ connected to input B-, and input A- connected to input B+) to form a bipolar input (except for board 59473-867-03).

Each input has an LED indicator that is on when the input is on (current flow from +IN to -IN terminals). Input circuit indicators are placed in sequence from 1 to 16 corresponding to inputs 1 to 16 (counting from the top of the board down). The board has two other indicators: the first one (the top one of the two located in the middle of the board near the board edge) is on for about 100 ms when data is read from the board. The second one (the lower of the two in the middle of the board) is on for about 100 ms when data is written to the board. These indicators flash once each second when the system is operating normally.

Each DI board interfaces with the data bus through a signature header. This signature header is created on the boards by a programming plug inserted in the socket labeled IC35. When a system is configured, a specific signature is assigned to each input slot. If an input board is changed, the correct signature must be inserted in the new board for that slot. The correct signature for that slot is listed on the module cover. The Alstom drawing number for the signature header is 59473-871 (see Appendix A for more information).

Figure 7–1 shows a DI board block diagram. The input circuitry provides a means of safely reading the presence of a DC voltage at the field terminals of the input and converting it to a form usable by the main processing system. In the same way that a Vital relay makes its front contacts if, and only if, power is applied to its coil, this input circuitry allows its true, or on, status to be displayed to the main processor (via a digital word) if, and only if, power is applied to its input terminals. In this scheme, all circuit failures result in the input being interpreted as off (or false), which is the more restrictive condition.

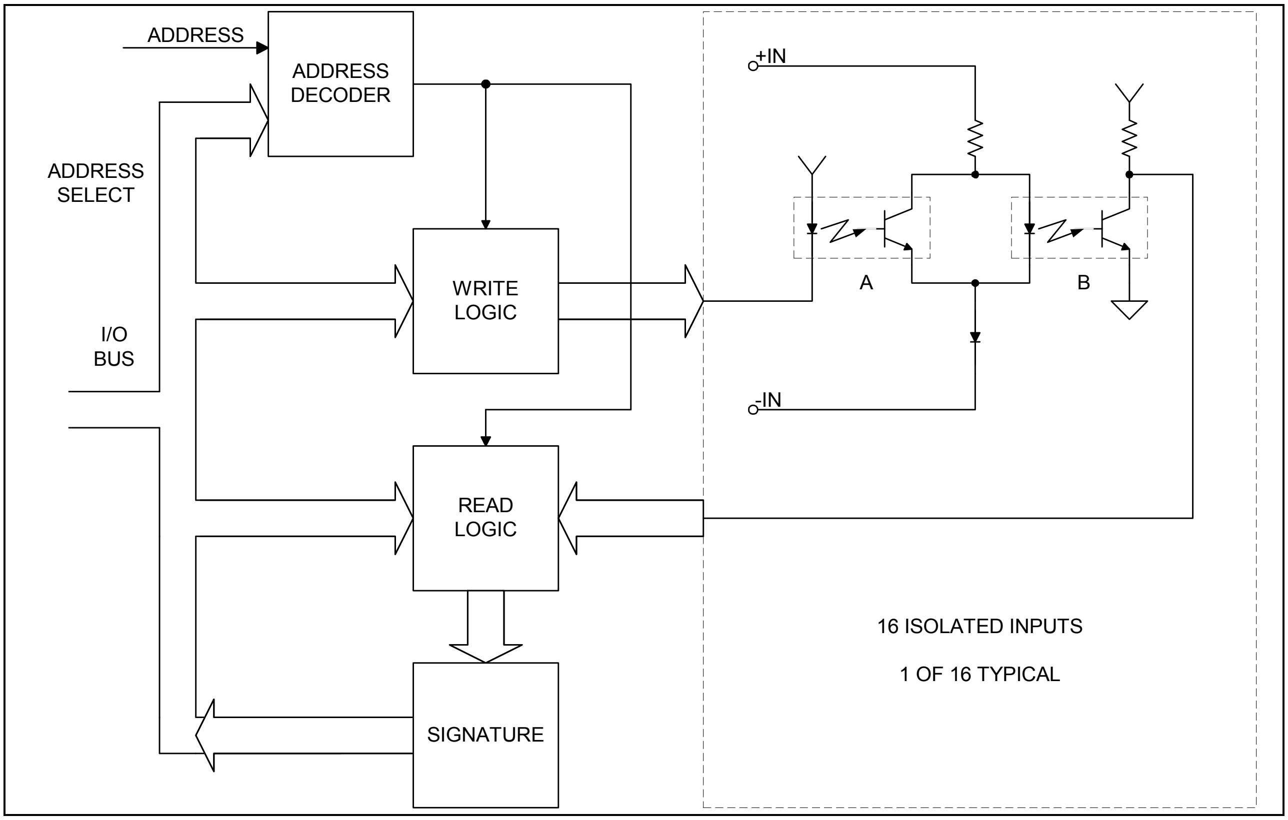

Figure 7–1. DI Board Block Diagram

All 16 inputs on a DI board are read at once by sending a serial bit stream to each input, one bit at a time, and then reading the results. The system outputs the first bit of the serial bit stream to each of the 16 inputs. It then reads the result of these bits at the output of each of the 16 inputs. Then the system outputs the second bit until the entire bit stream has been sent to the inputs and the results read back. The resultant bit pattern, called a word, represents the status of that input. The serial bit streams sent to the inputs are unique for each input and, therefore, the word that results (when an input is on) is unique for that input. For an input that is off, the returned word contains all zeroes.

Since this is a serial process, the resultant data is presented to the main processor in a serial form. The main processor cannot efficiently use the data in this form. Therefore, the resultant data is stored in shift registers on the I/O bus interface board and then is read by the main processor in a parallel process. This process is done in 8-bit segments because the shift registers are 8 bits long. Thus, the first 8 bits of the serial-bit stream are transmitted to the inputs one bit at a time and the resultant bits are stored in the shift registers.

Special attention is given to the reading of input checkwords to prevent induced AC from causing incorrect input sensing. This AC noise immunity is obtained by vitally spacing the reading of adjacent 8-bit segments of the 32-bit checkwords. Spacings of 7, 12 and 7 ms between 8-bit segments 1-2, 2-3 and 3-4 (respectively) are used.

Each input is read twice using two different 32-bit words (one word for each of the two processing channels). At the completion of this operation, only those inputs that are sensing current produce the correct 32-bit word in both channels for the CPU to use in evaluating the expressions.

7.3. OPERATION

The presence of a ‘0’, or low, on the write logic output line(s) causes opto-isolator A to turn on, see the block diagram in Figure 7–1. When this isolator turns on, its output transistor effectively diverts the current away from the input of opto-isolator B, causing its output to turn off. This in turn places a ‘1’, or high, on the input to the read logic. Similarly, if the write logic output is a ‘1’, the resultant input to the read logic is ‘0’. If there is no current flow (from the field) between the +IN and -IN terminals, then there is no current at the input of opto-isolator B to be diverted to the output transistor of isolator A. Thus, the output of isolator B remains in a high ‘1’ state all the time. Because the circuit has additional transistor stages, the returned data for an “off” input contains all zeros. The field input for each of these inputs contains a low-pass filter comprised of a 22 mFd capacitor and a 267Ω resistor. The purpose of this filter is to attenuate induced AC signals.

7.4. INDICATORS

Figure 7–2 shows the 18 DI board LED indicators. The sixteen input indicators (IN#) are driven directly from the voltage supplied to the input terminals. This provides a quick way to verify the state of an input.

DI BOARD
59473-867-XX

NORMAL INDICATION	PCB NOTATION	FUNCTION
OFF, ON	CR3	IN#1 (Input #1)
OFF, ON	CR5	IN#2 (Input #2)
OFF, ON	CR6	IN#3 (Input #3)
OFF, ON	CR8	IN#4 (Input #4)
OFF, ON	CR10	IN#5 (Input #5)
OFF, ON	CR11	IN#6 (Input #6)
OFF, ON	CR13	IN#7 (Input #7)
OFF, ON	CR15	IN#8 (Input #8)
FLASHING, BUT MOSTLY OFF	CR17	RD (Data Is Being Read From Input Board)
FLASHING, BUT MOSTLY OFF	CR18	WR (Data Is Being Written To The Input Board)
	TP4	COM (Common Test Point)
	TP5	DR (Test Point)
OFF, ON	CR21	IN#9 (Input #9)
OFF, ON	CR23	IN#10 (Input #10)
OFF, ON	CR24	IN#11 (Input #11)
OFF, ON	CR26	IN#12 (Input #12)
OFF, ON	CR28	IN#13 (Input #13)
OFF, ON	CR29	IN#14 (Input #14)
OFF, ON	CR31	IN#15 (Input #15)
OFF, ON	CR33	IN#16 (Input #16)

The above LEDS light when energy is applied to external input.

Figure 7–2. DI Board Edge

7.5. ADDRESS SIGNATURE HEADER

Appendix A lists the address signature headers' drawing number and signature letter used for board address definition with the VPI system.

7.6. TEST POINTS

Table 7–1 lists the DI board test points and Figure 7–3 shows the test point locations.

Table 7–1. DI Board Test Points

Test Points	
TP1	AD, board addressed for read or write function
TP2	SN, read operation to board
TP3	+5V, power
TP4	COM, common
TP5	DR, write operation to board

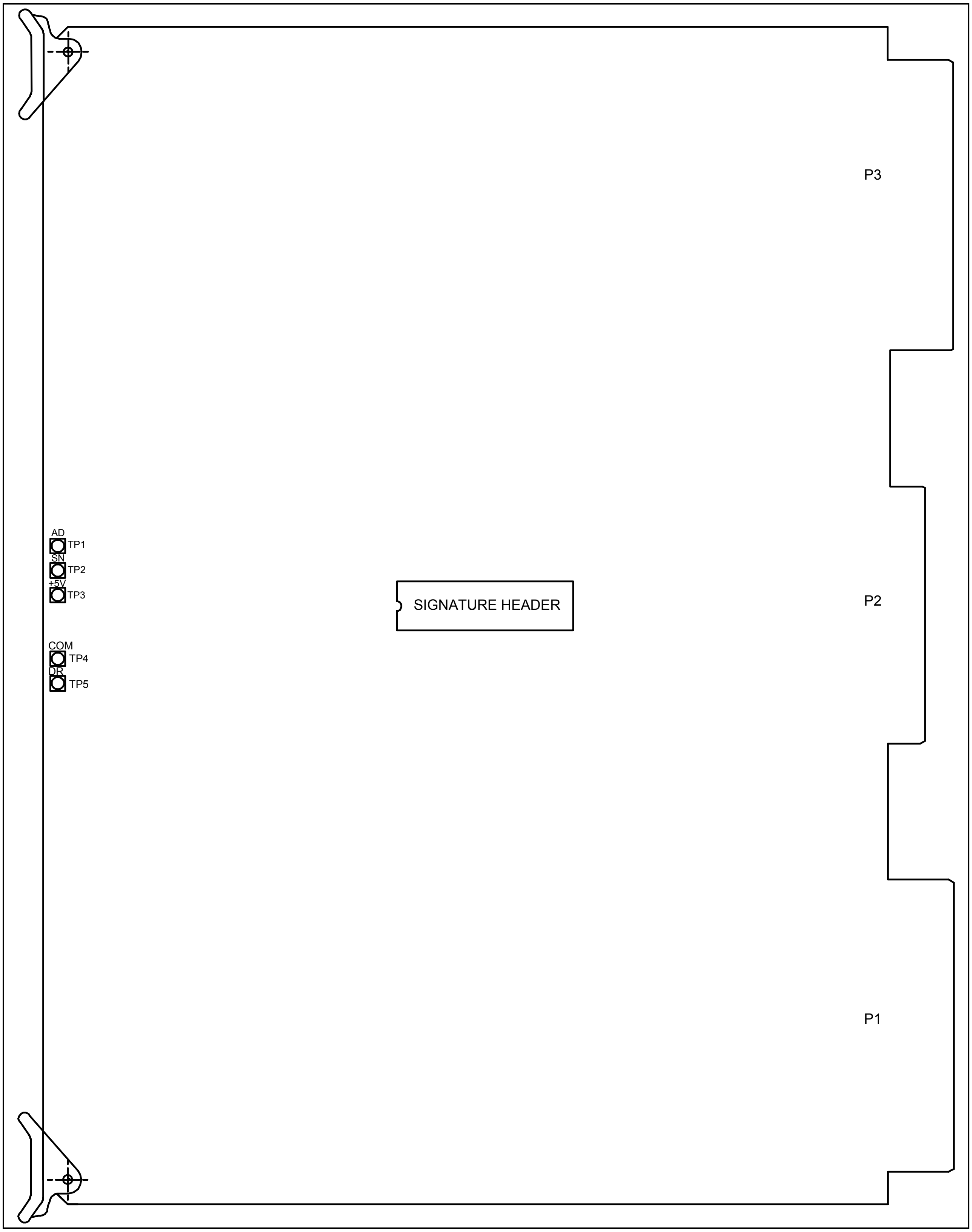

Figure 7–3. DI Board Test Points and Signature Header Locations

7.7. CARD EDGE CONNECTORS

The DI Board has three card edge connectors.

- P3, the top connector, is a 36-pin connector that connects inputs 1 through 8
  - See Table 7–2 for 36-pin configuration details
- P2, the middle connector, is a 50-pin connector that carries power, address and Vital I/O data
  - P 2-44 through P2-47 are wired in a specific pattern to common P2-48 per the application .lvc CAAPE report for board addressing; the remaining P2 pins are not user configurable
- P1, the lower connector, is a 36-pin connector that connects inputs 9 through 16
  - See Table 7–3 for 36-pin configuration details

Table 7–2. DI Board 36-pin P3 Connections

P3-	Name	Function
1	IN-8	Input 8 - V
2	IN+8	Input 8 +V
3		(not used)
4		(not used)
5	IN-7	Input 7 - V
6	IN+7	Input 7 +V
7		(not used)
8		(not used)
9	IN-6	Input 6 - V
10	IN+6	Input 6 +V
11		(not used)
12		(not used)
13	IN-5	Input 5 - V
14	IN+5	Input 5 +V
15		(not used)
16		(not used)
17	IN-4	Input 4 - V
18	IN+4	Input 4 +V
19		(not used)
20		(not used)
21	IN-3	Input 3 - V
22	IN+3	Input 3 +V
23		(not used)
24		(not used)
25	IN-2	Input 2 - V
26	IN+2	Input 2 +V
27		(not used)
28		(not used)
29	IN-1	Input 1 - V
30	IN+1	Input 1 +V
31-36		(not used)

Table 7–3. DI Board 36-pin P1 Connections

P1-	Name	Function
1	IN-16	Input 16 - V
2	IN+16	Input 16 +V
3		(not used)
4		(not used)
5	IN-15	Input 15 - V
6	IN+15	Input 15 +V
7		(not used)
8		(not used)
9	IN-14	Input 14 - V
10	IN+14	Input 14 +V
11		(not used)
12		(not used)
13	IN-13	Input 13 - V
14	IN+13	Input 13 +V
15		(not used)
16		(not used)
17	IN-12	Input 12 - V
18	IN+12	Input 12 +V
19		(not used)
20		(not used)
21	IN-11	Input 11 - V
22	IN+11	Input 11 +V
23		(not used)
24		(not used)
25	IN-10	Input 10 - V
26	IN+10	Input 10 +V
27		(not used)
28		(not used)
29	IN-9	Input 9 - V
30	IN+9	Input 9 +V
31-36		(not used)

7.8. SPECIFICATIONS / ASSEMBLY DIFFERENCES

Table 7–4. DI Board Specifications/Assembly Differences

Specification	**59473**					
	-867-01	**-867-02**	**-867-03**	**-867-04**	**-867-05**	**-867-07**
Maximum Number of Boards Per VPI System	20					
Board Slots Required	1					
Maximum Board Logic Current Supply	300 mA					
Minimum Input Voltage/Port	9.0 VDC	9.0 VDC	9.0 VDC	45.0 VDC	9.0 VDC	24.0 VDC
Maximum Input Voltage/Port	15.0 VDC	15.0 VDC	15.0 VDC	55.0 VDC	22.0 VDC	34.0 VDC
Input Transient Protection Voltage (Max Voltage)	1700 Vrms					
Input Transient Protection Energy (Max Energy)	3.6 Joules					
Isolation Between Inputs	> 3000 Vrms					
Address Signature Header Required	Yes					
Equipped with Low-Pass Filter	Yes	No	No	Yes	Yes	Yes
Momentary Input Hold	No	No	Yes (see Warning)	No	No	No

WARNING

THE 59473-867-03 ASSEMBLY INPUT CIRCUIT POSSESSES THE ABILITY TO RECTIFY AC SIGNALS AND IS INTENDED FOR SPECIAL SITUATIONS ONLY. CONSULT ALSTOM ON ITS USE.

8. SECTION 8 – VITAL DC OUTPUT BOARDS, P/N 59473-739-XX, -747-XX, -977-XX, -749-XX, 31166-340-XX

8.1. INTRODUCTION

This section provides Vital DC output board detail.

8.2. GENERAL

There are five types of Vital DC Output boards: Single Break Output (SBO) P/N 59473-739-XX, Double Break Output (DBO) P/N 59473-747-XX, Double Break Output 50 V (DBO-50V) P/N 59473-977-XX, Lamp Driver Output (LDO) P/N 59473-749-XX, and Lamp Driver Output 2 (LDO2) P/N 31166-340-XX. All are configured with 8 Vital outputs per board. The single break output is analogous to a single relay contact placed in the positive or feed side of the circuit. The equivalent to the relay contact in the solid state circuit is the FET switch. The double break output is analogous to a relay circuit with the contacts in both the feed and return sides of the circuit. With the solid-state equivalent, however, each output is completely isolated from all other outputs and/or power supplies.

WARNING

BOARD SPECIFICATION TABLES ARE PROVIDED IN THE INDIVIDUAL OUTPUT BOARD DISCUSSIONS. EACH TABLE INCLUDES THE MINIMUM REQUIRED APPLICATION LOAD CURRENT DATA SPECIFIC TO THAT BOARD. THIS SPECIFICATION MUST BE FOLLOWED FOR THE BOARD TO FUNCTION PROPERLY.

8.3. OPERATION

Ten LED indicators are on each output board. The top indicator lights for about 50 ms every time data is read from the board. Under normal conditions, this indicator appears to be “on” all the time because the main processing system reads the output check data from the output boards every 50 ms. The second indicator lights for 50 ms every time data is written to this board. Since the system does this once per second (twice for flashing outputs), this indicator flashes once or twice per second under normal conditions. The remaining 8 indicators represent the status of the 8 outputs. Each indicator lights only when the system requests the associated output to turn on. The third indicator from the top of the board is for output number 1 and the last indicator on the board is for output number 8.

Eight outputs on each board are divided into two groups of four. Outputs 1-4 are connected to one power supply input, while outputs 5-8 are connected to a second power supply input. These power supply inputs may be connected to different power supplies or they may be tied together external to the VPI module. If the outputs are being used in a Vital application, the power supply must come from a source that can be vitally turned off (usually a contact of the VPI Vital relay or one of its repeaters).

Each output board is assigned a Signature PROM (see Appendix A for more information) that contains a unique set of data for each of the outputs on that board. These data are tied into the board addressing and are used to prove that there are no addressing failures. They are also used by the output check circuitry to prove the status of the output. When an output board is changed, this PROM must be changed to the new board. If an output board is missing its PROM or contains a wrong PROM, the system does not operate.

Figure 8–1 shows a block diagram of the Vital DC Output boards.

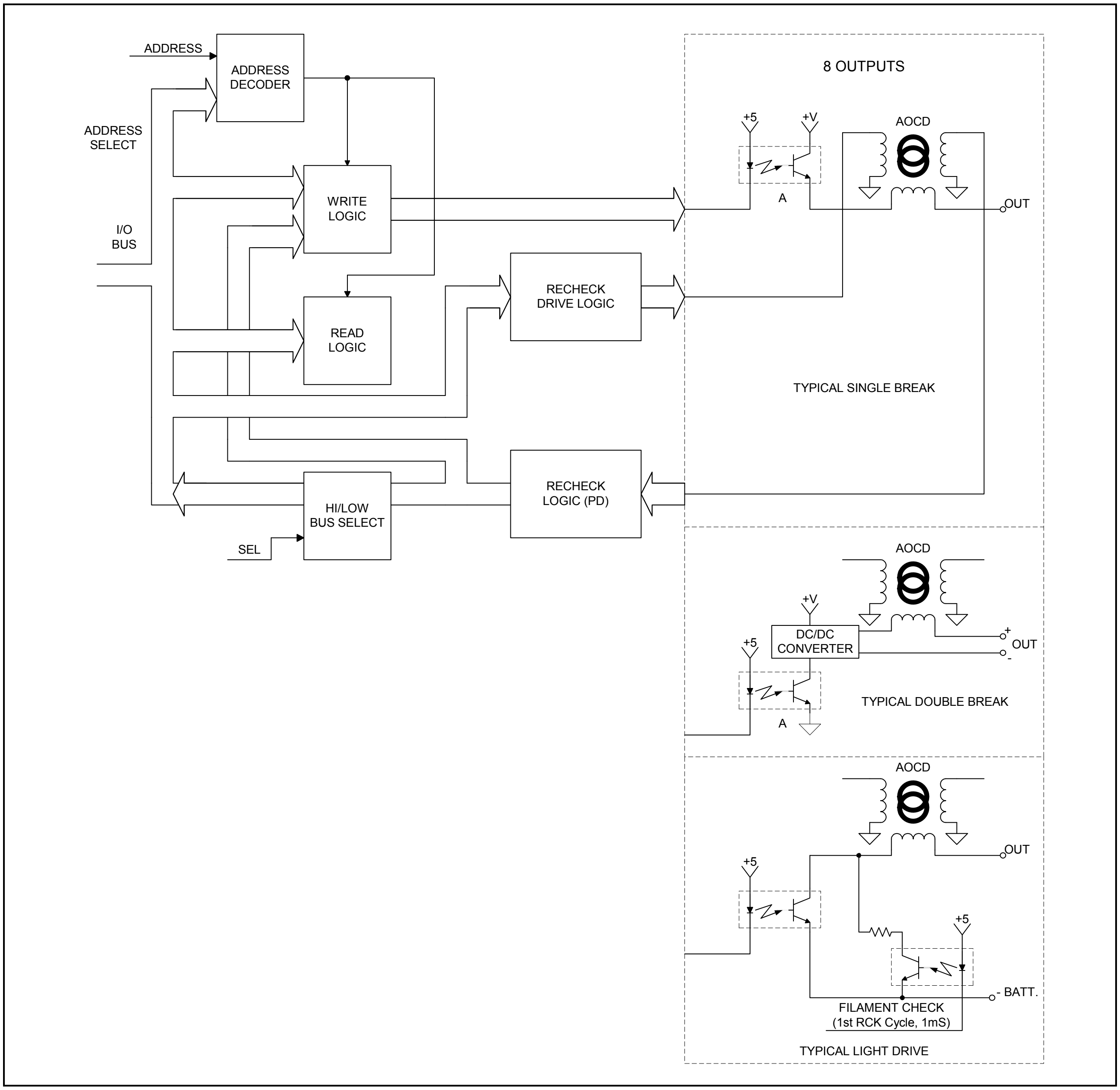

Figure 8–1. Vital DC Output Board Block Diagram

For these boards, the outputs are turned “on” by writing a ‘1’ to the output and turned “off” by writing a ‘0’. The main processing system controls the status of the outputs by setting the data bus lines to the data pattern corresponding to the desired output on/off status and writing that data to the output board. Since the system has a 16-bit wide data bus, 16 outputs can be updated at once.

To accomplish this, two output boards are given the same address and:

- one board is connected to the lower half of the data bus
- one board is connected to the upper half

For the board on the lower half of the bus, output 1 corresponds to data bus line 0 and output 8 to data bus line 7. For the board on the upper half, output 1 corresponds to data line 8 and output 8 is data line F.

Besides turning the outputs on and off, the VPI system checks each output to ensure it is in the correct state. To do this, each output circuit monitors its output current flow. This circuitry, called an Absence Of Current Detector (AOCD), passes a digital signal if, and only if, the current in its output winding is less than a specified level.

Each output board contains the necessary logic to circulate a digital word through the AOCD, read the resultant word at the output of the AOCD, divide it by a preset polynomial, and store the result. Every 50 ms the main processor reads the result of this process. If the output is in the off state, the result indicates that there was no current flow for the entire 50 ms period.

WARNING

> VPI USERS MUST CONFIRM THAT OUTPUT DEVICE CURRENT REQUIREMENTS ARE CONSISTENT WITH AOCD CURRENT THRESHOLD CHARACTERISTICS.

A systematic breakdown of this circuit's operation follows:

- Each output board has a unique signature header that is a 32 × 8 PROM (39780-003-XX). The PROM contains 8 32-bit words arranged vertically. These words are clocked serially through the AOCD associated with each output at a rate of 1 bit every 128 μs.
- The 32-bit word is cycled through the output's AOCD 11 consecutive times. This requires 11 × 32 × 128 μs = 45,056 μs.
- All serial data streams circulated through each of the 8 AOCDs are compressed into 8 32-bit words in RAM (which is made up from two 256 × 4 RAMs). The compressed data appear vertically in the RAM.
- The data are compressed via 8 individual polynomial dividers that operate simultaneously; each polynomial has an even and an odd cycle, they alternate as a set between even and odd every 50 ms (they are all even or all odd at once)

- At the end of a verification cycle the value of a particular 32-bit vertical result in RAM is the correct value if, and only if both of the following two statements are true:
  - there were no failures in the AOCD circuitry
  - the current in the AOCD output winding was below the specified threshold for the entire verification period
- For a given output, the unique 32-bit result depends on the polynomial used during the verification cycle:
  - the polynomial used is pe(x) for even 50 ms recheck cycles and po(x) for odd 50 ms recheck cycles
  - by using different polynomials on adjacent recheck cycles, it proves that the 32-bit result was calculated during the current 50 ms and not left over from a previous recheck period
- The data compression in RAM is accomplished by manipulating the RAM to simulate a 32-bit feedback shift register that represents the desired polynomial

The RAM address PROM is 512 × 8 and it is divided into four 128 × 8 sections. Two of the sections contain the address sequences that represent the two diverse primitive polynomials. The remaining two sections contain the address sequences needed to read the collected compressed data from the RAM and the sequence needed to initialize the RAM to all “ones”. The RAM is initialized at the beginning of each recheck cycle.

Control logic for synchronizing and clocking this circuitry is contained on the I/O Bus Interface board.

Operation of this circuitry is divided into four modes:

1. READ MODE: In the read mode, the data from the RAM is read. Since the read data is stored vertically in RAM, each group of 8 bits represents one bit of each of the 8 words. This data is serially clocked into shift registers on the I/O Bus Interface board. Each shift register receives one bit for each read operation. After 8 read operations, a particular shift register contains 8 of the 32 bits of a particular output's checkword. The shift register data is then stored in the CPU memory. This process continues until the entire 32-bit word is read and stored for all the outputs.

2. WRITE MODE: In this mode, the RAM is filled with all “ones”.

3. CIRCULATE MODE (11): In this mode, the even or odd polynomial is selected depending on which recheck cycle is in process and the 32-bit words are cycled through the AOCD circuitry 11 times.

4. CIRCULATE MODE (1): This mode circulates the first 8 bits of the 32-bit word through the AOCD circuitry and then stops. This allows the state of the output to be changed, after which circulate mode 11 is invoked to complete the recheck cycle. Special tests can be run on selected outputs, such as a hot or cold lamp filament check. The returned 32-bit word obtained by this mode of operation is unique and indicates that the desired test was performed correctly.

NOTE

When this test is required for current and filament checking, a wire wrap jumper is installed between pins 35 and 36 on the Motherboard in the slot for that output board.

8.4. INDICATORS

Figures 8–2 through 8–6 show the SBO, DBO, DBO-50, LDO, and LDO2 board edges, including LED indicators.

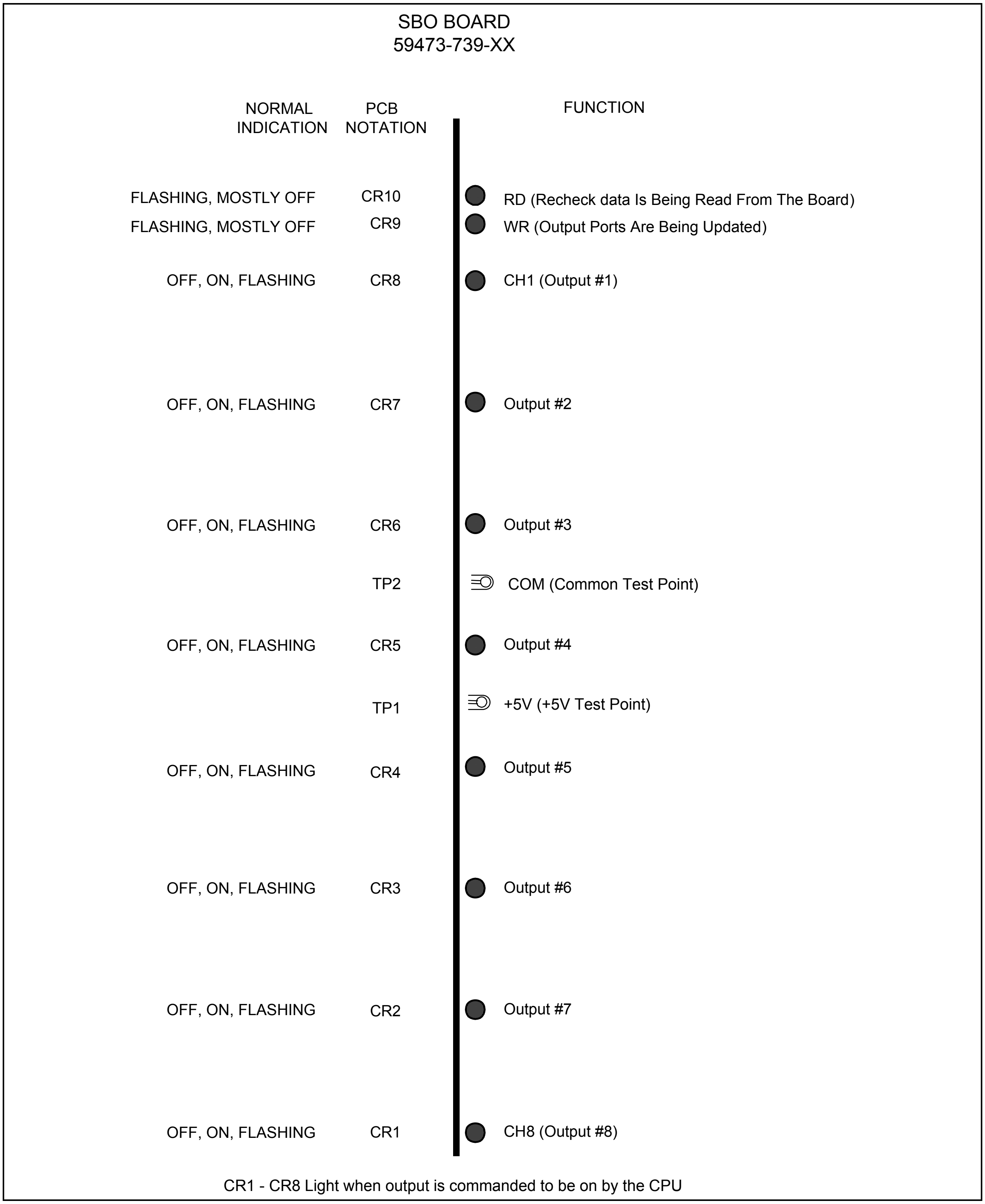

Figure 8–2. Vital Output SBO Board Edge

DBO BOARD
59473-747-XX

NORMAL INDICATION	PCB NOTATION	FUNCTION
FLASHING, MOSTLY OFF	CR1	RD (Recheck data Is Being Read From The Board)
FLASHING, MOSTLY OFF	CR2	WR (Output Ports Are Being Updated)
OFF, ON, FLASHING	CR10	CH1 (Output #1)
OFF, ON, FLASHING	CR9	Output #2
OFF, ON, FLASHING	CR8	Output #3
OFF, ON, FLASHING	CR7	Output #4
OFF, ON, FLASHING	CR6	Output #5
OFF, ON, FLASHING	CR5	Output #6
OFF, ON, FLASHING	CR4	Output #7
	TP7	+5V (+5V Test Point)
	TP8	COM (Common Test Point)
OFF, ON, FLASHING	CR3	CH8 (Output #8)

CR3 - CR10 Light when output is commanded to be on by the CPU.

Figure 8–3. Vital Output DBO Board Edge

DBO-50V BOARD
59473-977-XX

NORMAL INDICATION	PCB NOTATION	FUNCTION
FLASHING, MOSTLY OFF	CR1	RD (Recheck data Is Being Read From The Board)
FLASHING, MOSTLY OFF	CR2	WR (Output Ports Are Being Updated)
OFF, ON, FLASHING	CR3	CH1 (Output #1)
OFF, ON, FLASHING	CR4	Output #2
OFF, ON, FLASHING	CR5	Output #3
	E1	+5V (+5V Test Point)
OFF, ON, FLASHING	CR6	Output #4
	E2	COM (Common Test Point)
OFF, ON, FLASHING	CR7	Output #5
OFF, ON, FLASHING	CR8	Output #6
OFF, ON, FLASHING	CR9	Output #7
OFF, ON, FLASHING	CR10	CH8 (Output #8)

CR3 - CR10 Light when output is commanded to be on by the CPU.

Figure 8–4. Vital Output DBO-50V Board Edge

LDO BOARD
59473-749-XX

NORMAL INDICATION	PCB NOTATION	FUNCTION
FLASHING, MOSTLY OFF	CR1	RD (Recheck data Is Being Read From The Board)
FLASHING, MOSTLY OFF	CR2	WR (Output Ports Are Being Updated)
OFF, ON, FLASHING	CR10	CH1 (Output #1)
OFF, ON, FLASHING	CR9	Output #2
OFF, ON, FLASHING	CR8	Output #3
OFF, ON, FLASHING	CR7	Output #4
	TP2	COM (Common Test Point)
OFF, ON, FLASHING	CR6	Output #5
OFF, ON, FLASHING	CR5	Output #6
	TP1	+5V (+5V Test Point)
OFF, ON, FLASHING	CR4	Output #7
OFF, ON, FLASHING	CR3	CH8 (Output #8)

CR3 - CR10 Light when output is commanded to be on by the CPU.

Figure 8–5. Vital Output LDO Board Edge

LDO2 BOARD
31166-340-XX

NORMAL INDICATION	PCB NOTATION	FUNCTION
OFF	DS1	ERROR (Error)
	S3	CLEAR (Clear Switch)
	S5	Toggle Switch
	DS2	Output Number Display
	DS3	Parameter Data Display
	DS4	Parameter Data Display
OFF,ON, FLASHING	DS5	OUT1 (Output #1)
OFF,ON, FLASHING	DS6	OUT2 (Output #2)
OFF,ON, FLASHING	DS7	OUT3 (Output #3)
OFF,ON, FLASHING	DS8	OUT4 (Output #4)
OFF,ON, FLASHING	DS9	OUT5 (Output #5)
OFF,ON, FLASHING	DS10	OUT6 (Output #6)
OFF,ON, FLASHING	DS11	OUT7 (Output #7)
OFF,ON, FLASHING	DS12	OUT8 (Output #8)
	S13	RESET (Reset Switch)
OFF when configuration is complete	DS13	CONFIG (Config Is Being Accessed)

Figure 8–6. Vital Output LDO2 Board Edge

8.5. SBO DETAILS

The single break output is analogous to a single relay contact placed in the positive or feed side of the circuit. The equivalent of the relay contact in the solid-state circuit is the FET switch. Figure 8–7 shows the SBO board block diagram.

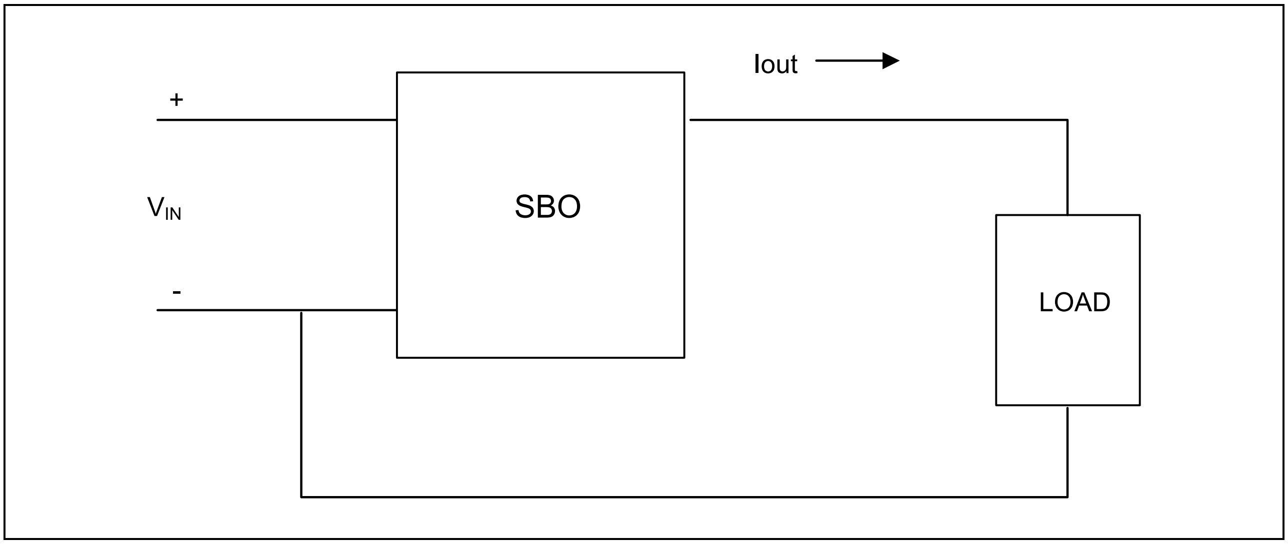

Figure 8–7. Single Break Output Block Diagram

8.5.1. SBO Board Test Points

Table 8–2 lists the SBO board test points and Figure 8–8 shows the test point locations.

Table 8–1. SBO Board Test Points

Test Points	
TP1	+5V, power
TP2	COM, common
TP3, TP4, TP5 TP6, TP7, TP8, TP9	used for factory test

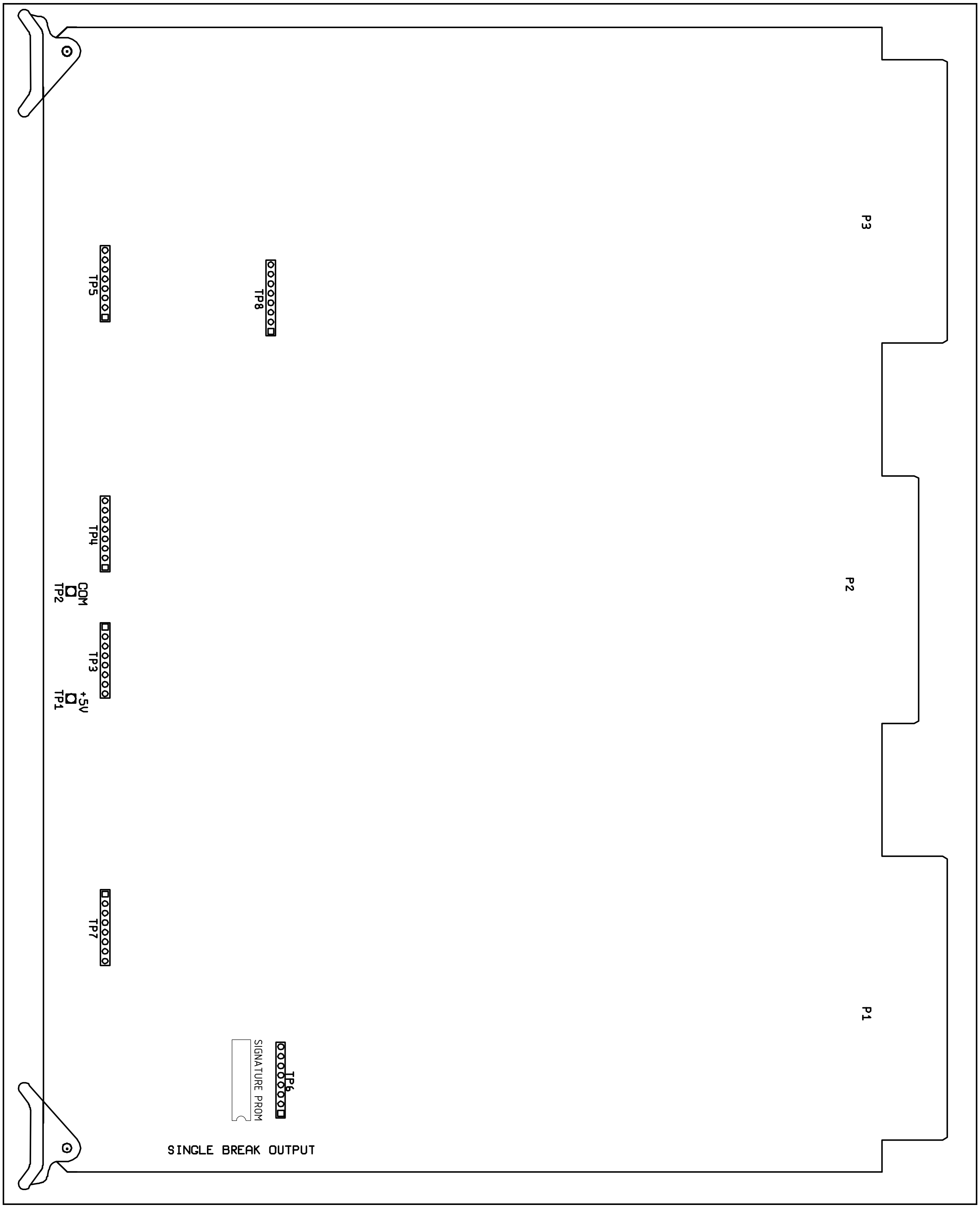

Figure 8–8. SBO Board Test Point and Signature PROM Locations

8.5.2. Card Edge Connectors

The SBO Board has three card edge connectors.

- P3, the top connector, is a 36-pin connector for Channels 1 through 4
  - See Table 8–2 for 36-pin configuration details
- P2, the middle connector, is a 50-pin connector that carries power, address and Vital I/O data
  - P2-42 or P2-43 are wired to P2-40 and P2-44 through P2-47 are wired in a specific pattern to common P2-48 per the application .lvc CAAPE report for board addressing; the remaining P2 pins are not user configurable
- P1, the lower connector, is a 36-pin connector for Channels 5 through 8
  - See Table 8–3 for 36-pin configuration details

Table 8–2. SBO Board 36-pin P3 Connections

P3-	Name	Function
1	OUTV1COM	Vital Power Common
2	+OUT4	Output 4
3 - 8		(not used)
9	OUTV1COM	Vital Power Common
10	+OUT3	Output 3
11 - 20		(not used)
21	OUTV1COM	Vital Power Common
22	+OUT2	Output 2
23		(not used)
24		(not used)
25	OUTV1COM	Vital Power Common
26	+OUT1	Output 1
27 - 32		(not used)
33	OUTV1COM	Vital Power Common
34	+V1	Vital Power V+
35		(not used)
36		(not used)

Table 8–3. SBO Board 36-pin P1 Connections

P1-	Name	Function
1	OUTV2COM	Vital Power Common
2	+OUT8	Output 8
3 - 8		(not used)
9	OUTV2COM	Vital Power Common
10	+OUT7	Output 7
11 - 20		(not used)
21	OUTV2COM	Vital Power Common
22	+OUT6	Output 7
23		(not used)
24		(not used)
25	OUTV2COM	Vital Power Common
26	+OUT5	Output 7
27 - 32		(not used)
33	OUTV2COM	Vital Power Common
34	+V2	Vital Power V+
35		(not used)
36		(not used)

8.5.3. Specifications/Assembly Differences

Table 8–4. SBO Board Specifications/Assembly Differences

Specification	**59473-739**	
	-01	**-02**
Maximum Number of Boards Per VPI System	40	
Board Slots Required	1	
Number of Ports per Board	8	
Maximum Board Logic Current Supply	500 mA	
Minimum Switched Output Supply Voltage (Vin)	9.0 VDC	
Maximum Switched Output Supply Voltage (Vin)	30.0 VDC	
Typical Output Voltage Drop	1.0 VDC	
Maximum Switched Power	15 watts	
AOCD Current Threshold	3 mA max	
Maximum Output Current Per Port (Iout)	500 mA	
Isolation Between Outputs and 5 Volt Logic	> 3000 Vrms	
Address Signature PROM Required	Yes	
Code Energy Switching	No	Yes
Group Energy Filtered	Yes	No

WARNING

THE SBO BOARD MAY FAIL WITH UP TO 3 MILLIAMPERES OF OUTPUT LEAKAGE CURRENT WITH THE SYSTEM REQUESTING THE OUTPUT TO BE IN THE DE-ENERGIZED STATE. TO PREVENT A POTENTIAL UNSAFE CONDITION, ANY LOAD DEVICE ATTACHED TO A LOW CURRENT VITAL OUTPUT CIRCUIT BOARD MUST NOT OPERATE AND MUST DE-ACTIVATE ABOVE 3 MILLIAMPERES. THIS INCLUDES ALL ENVIRONMENTAL OPERATING CONDITIONS AND ALL OPERATING VALUES OF THE LOAD DEVICE OVER ITS SERVICE LIFE. FAILURE TO FOLLOW THIS REQUIREMENT MAY LEAD TO UNEXPECTED OPERATION OF THE LOAD DEVICE.

8.6. DBO AND DBO-50V DETAILS

The double break output is analogous to a relay circuit with the contacts in both the feed and return sides of the circuit. With the solid-state equivalent, however, each output is completely isolated from all other outputs and/or power supplies. Each output is isolated by using individual DC/DC converters that meet or exceed AREMA isolation requirement. Figure 8–9 shows the DBO board block diagram.

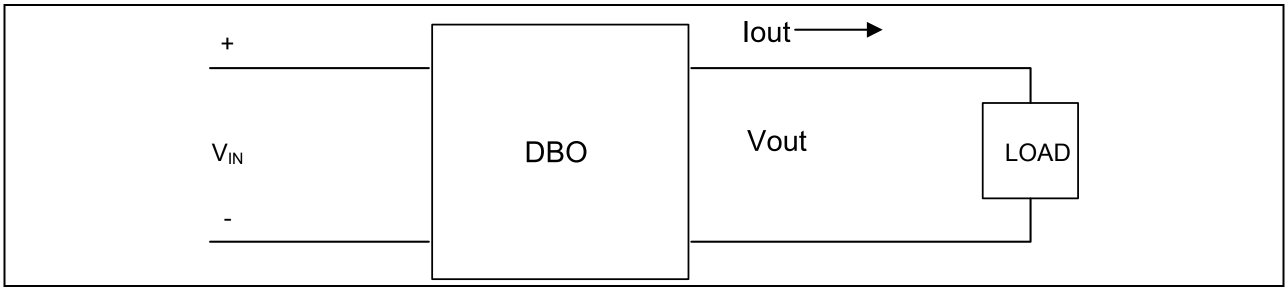

Figure 8–9. DBO Board Block Diagram

8.6.1. DBO and DBO-50V Board Test Points

See Figure 8–10 for DBO board test point locations and Figure 8–11 for DBO-50V board test point locations.

Table 8–5. DBO Board Test Points

Test Points	
TP1, TP2, TP3, TP4, TP5	used for factory test
TP7	+5V, power
TP8	COM, common

Table 8–6. DBO-50V Board Test Points

Test Points	
E1	+5V, power
E2	COM, common

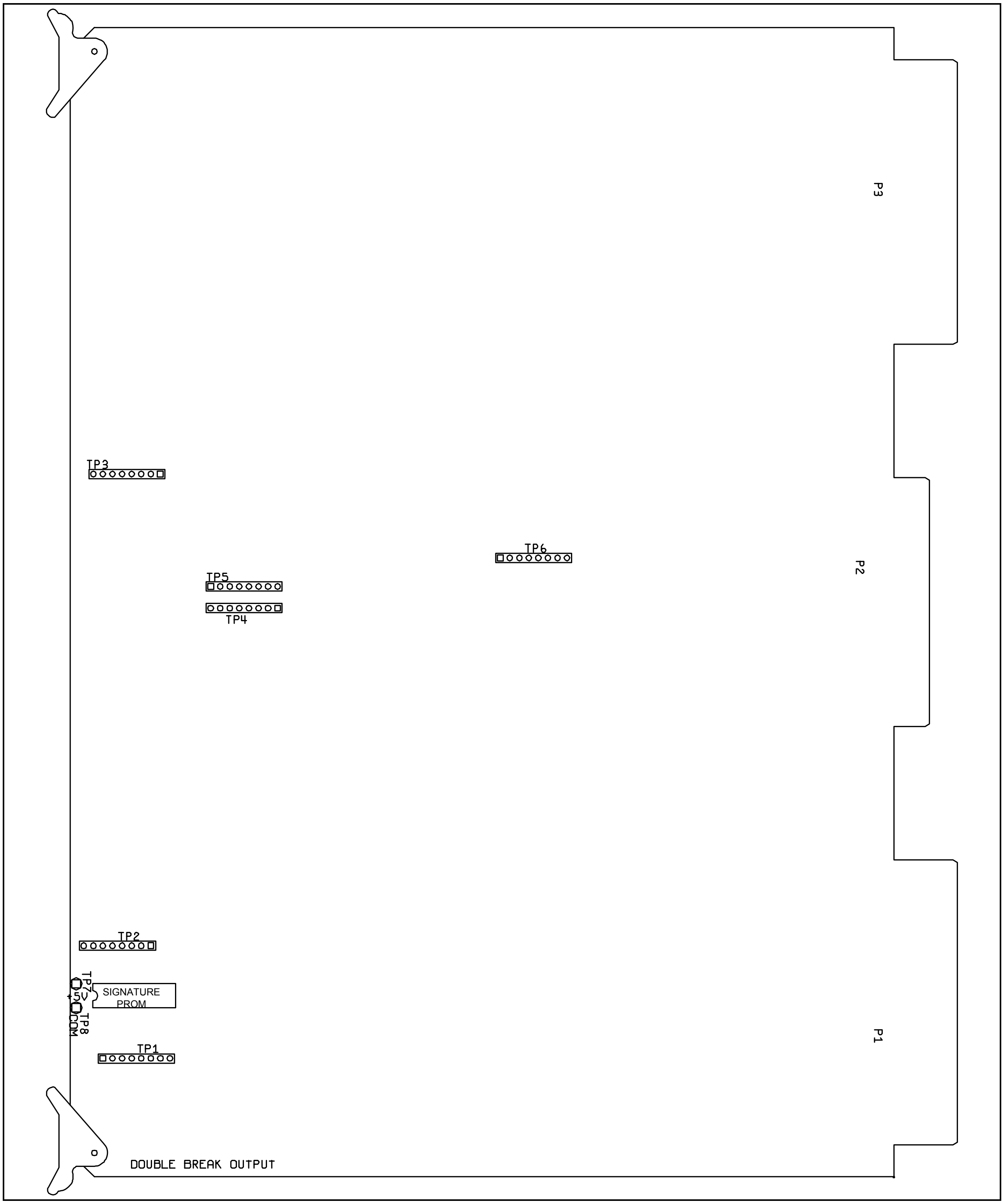

Figure 8–10. DBO Board Test Point and Signature PROM Locations

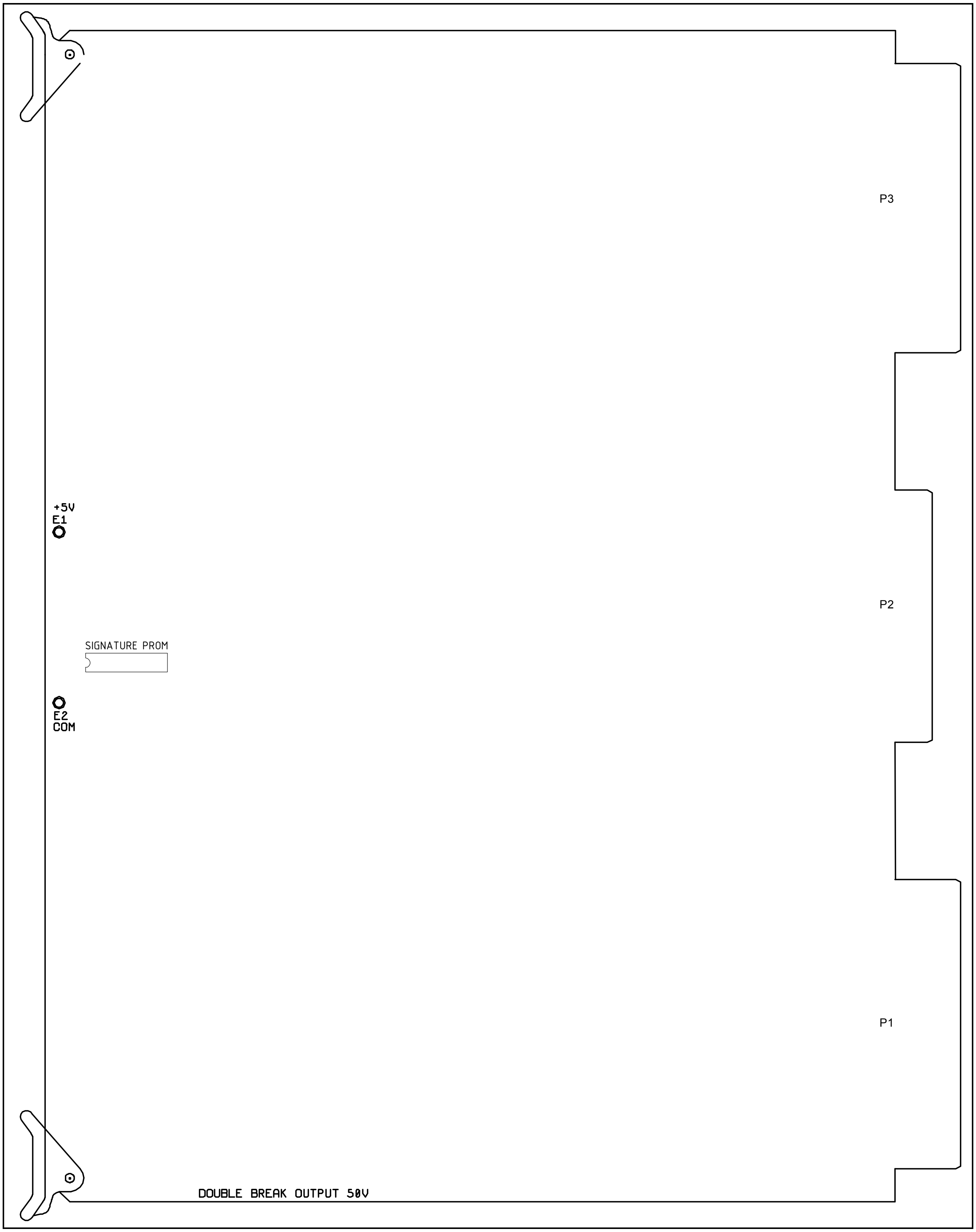

Figure 8–11. DBO-50V Board Test Point and Signature PROM Locations

8.6.2. Card Edge Connectors

The DBO and DBO-50 Boards have three card edge connectors.

- P3, the top connector, is a 36-pin connector for Channels 1 through 4
  - See Table 8–7 for DBO 36-pin configuration details
  - See Table 8–9 for DBO-50 36-pin configuration details
- P2, the middle connector, is a 50-pin connector that carries power, address and Vital I/O data
  - P2-42 or P2-43 are wired to P2-40 and P2-44 through P2-47 are wired in a specific pattern to common P2-48 per the application .lvc CAAPE report for board addressing; the remaining P2 pins are not user configurable
- P1, the lower connector, is a 36-pin connector for Channels 5 through 8
  - See Table 8–8 for DBO 36-pin configuration details
  - See Table 8–10 for DBO-50 36-pin configuration details

Table 8–7. DBO Board 36-pin P3 Connections

P3-	Name	Function
1	OUT4-	Output 4 -V
2	OUT4+	Output 4
3 - 8		(not used)
9	OUT3-	Output 3 -V
10	OUT3+	Output 3
11 - 20		(not used)
21	OUT2-	Output 2 -V
22	OUT2+	Output 2
23		(not used)
24		(not used)
25	OUT1-	Output 1 -V
26	OUT1+	Output 1
27 - 32		(not used)
33	OUTCOM1	Vital Power Common
34	OUTV1	Vital Power V+
35		(not used)
36		(not used)

Table 8–8. DBO Board 36-pin P1 Connections

P1-	Name	Function
1	OUT8-	Output 8 -V
2	OUT8+	Output 8
3 - 8		(not used)
9	OUT7-	Output 7 -V
10	OUT7+	Output 7
11 - 20		(not used)
21	OUT6-	Output 6 -V
22	OUT6+	Output 6
23		(not used)
24		(not used)
25	OUT5-	Output 5 -V
26	OUT5+	Output 5
27 - 32		(not used)
33	OUTCOM3	Vital Power Common
34	OUTV3	Vital Power V+
35		(not used)
36		(not used)

Table 8–9. DBO-50 Board 36-pin P3 Connections

P3-	Name	Function
1	OUT4-	Output 4 -V
2	OUT4+	Output 4
3 - 8		(not used)
9	OUT3-	Output 3 -V
10	OUT3+	Output 3
11 - 20		(not used)
21	OUT2-	Output 2 -V
22	OUT2+	Output 2
23		(not used)
24		(not used)
25	OUT1-	Output 1 -V
26	OUT1+	Output 1
27 - 32		(not used)
33	50VCOM1	Vital Power Common
34	V1	Vital Power V+
35		(not used)
36		(not used)

Table 8–10. DBO-50 Board 36-pin P1 Connections

P1-	Name	Function
1	OUT8-	Output 8 -V
2	OUT8+	Output 8
3 - 8		(not used)
9	OUT7-	Output 7 -V
10	OUT7+	Output 7
11 - 20		(not used)
21	OUT6-	Output 6 -V
22	OUT6+	Output 6
23		(not used)
24		(not used)
25	OUT5-	Output 5 -V
26	OUT5+	Output 5
27 - 32		(not used)
33	50VCOM2	Vital Power Common
34	V2	Vital Power V+
35		(not used)
36		(not used)

8.6.3. Specifications/Assembly Differences

Table 8–11. DBO/DBO-50 Board Specifications/Assembly Differences

Specification	59473			
	-747-02	**-747-03**	**-977-01**	**-977-02**
Maximum Number of Output Boards Per VPI System	40			
Board Slots Required	1			
Number of Ports Per Board	8			
Maximum Board Logic Current Supply	500 mA			
Minimum Input Voltage (Vin)	9.0 VDC	9.0 VDC	30.0 VDC	45.0 VDC
Maximum Input Voltage (Vin)	15.0 VDC	15.0 VDC	40.0 VDC	55.0 VDC
Minimum Output Voltage (Vout)	17.7 VDC	6.0 VDC	45.0 VDC	45.0 VDC
Maximum Output Voltage (Vout)	34.5 VDC	15.0 VDC	55.0 VDC	55.0 VDC
Maximum Output Current Per Port (Iout)	300 mA	600 mA	140 mA	140 mA
Maximum Output Power Per Port	9 W	9 W	7.7 W	7.7 W
AOCD Current Threshold	3 mA max	3 mA max	3 mA max	3 mA max
Isolation Between Outputs	> 3000 Vrms	> 3000 Vrms	> 3000 Vrms	> 3000 Vrms
Address Signature PROM Required	Yes	Yes	Yes	Yes

WARNING

THE DBO BOARD MAY FAIL WITH UP TO 3 MILLIAMPERES OF OUTPUT LEAKAGE CURRENT WITH THE SYSTEM REQUESTING THE OUTPUT TO BE IN THE DE-ENERGIZED STATE. TO PREVENT A POTENTIAL UNSAFE CONDITION, ANY LOAD DEVICE ATTACHED TO A LOW CURRENT VITAL OUTPUT CIRCUIT BOARD MUST NOT OPERATE AND MUST DE-ACTIVATE ABOVE 3 MILLIAMPERES. THIS INCLUDES ALL ENVIRONMENTAL OPERATING CONDITIONS AND ALL OPERATING VALUES OF THE LOAD DEVICE OVER ITS SERVICE LIFE. FAILURE TO FOLLOW THIS REQUIREMENT MAY LEAD TO UNEXPECTED OPERATION OF THE LOAD DEVICE.

8.7. LDO DETAILS

The lamp drive output circuit handles high current to light signal lamps. Each output circuit can accommodate hot and cold filament checks. This output uses a FET switch in the common or return line of the circuit. Therefore, it is necessary to supply the positive side of the battery or signal lighting supply to the signal lamps. Figure 8–12 shows the LDO board port interface block diagram.

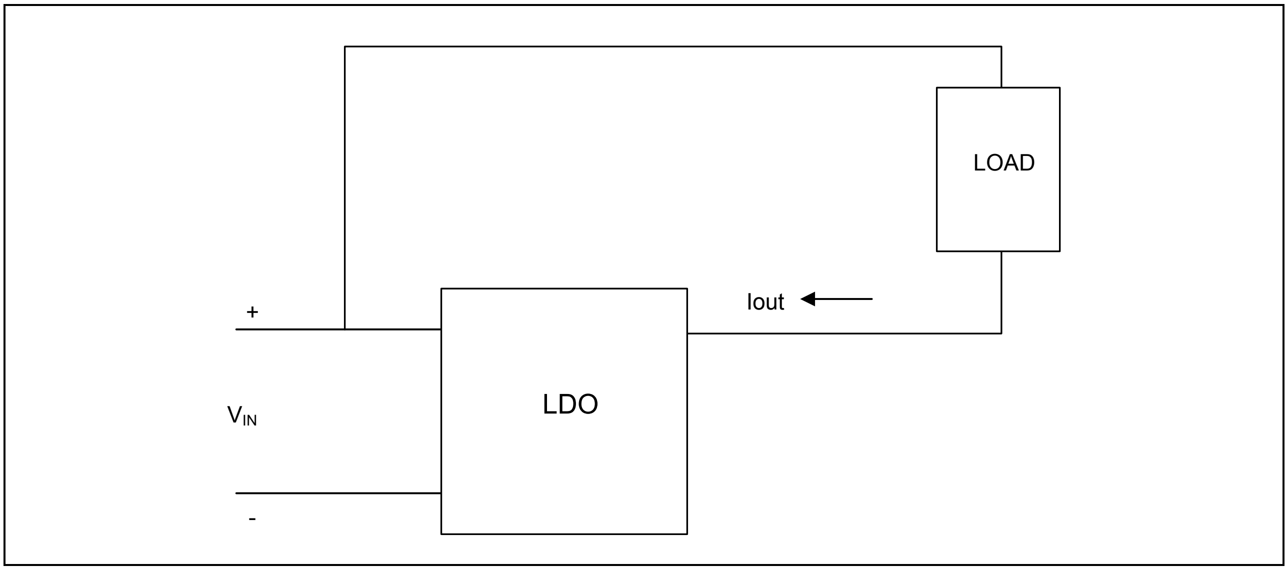

Figure 8–12. LDO Board Port Interface

8.7.1. LDO Board Test Points

Table 8–12 lists the LDO board test points and Figure 8–13 shows the test point locations.

Table 8–12. LDO Board Test Points

Test Points	
TP1	+5V, power
TP2	COM, common
TP3, TP4, TP5, TP6, TP7, TP8, TP9	used for factory test

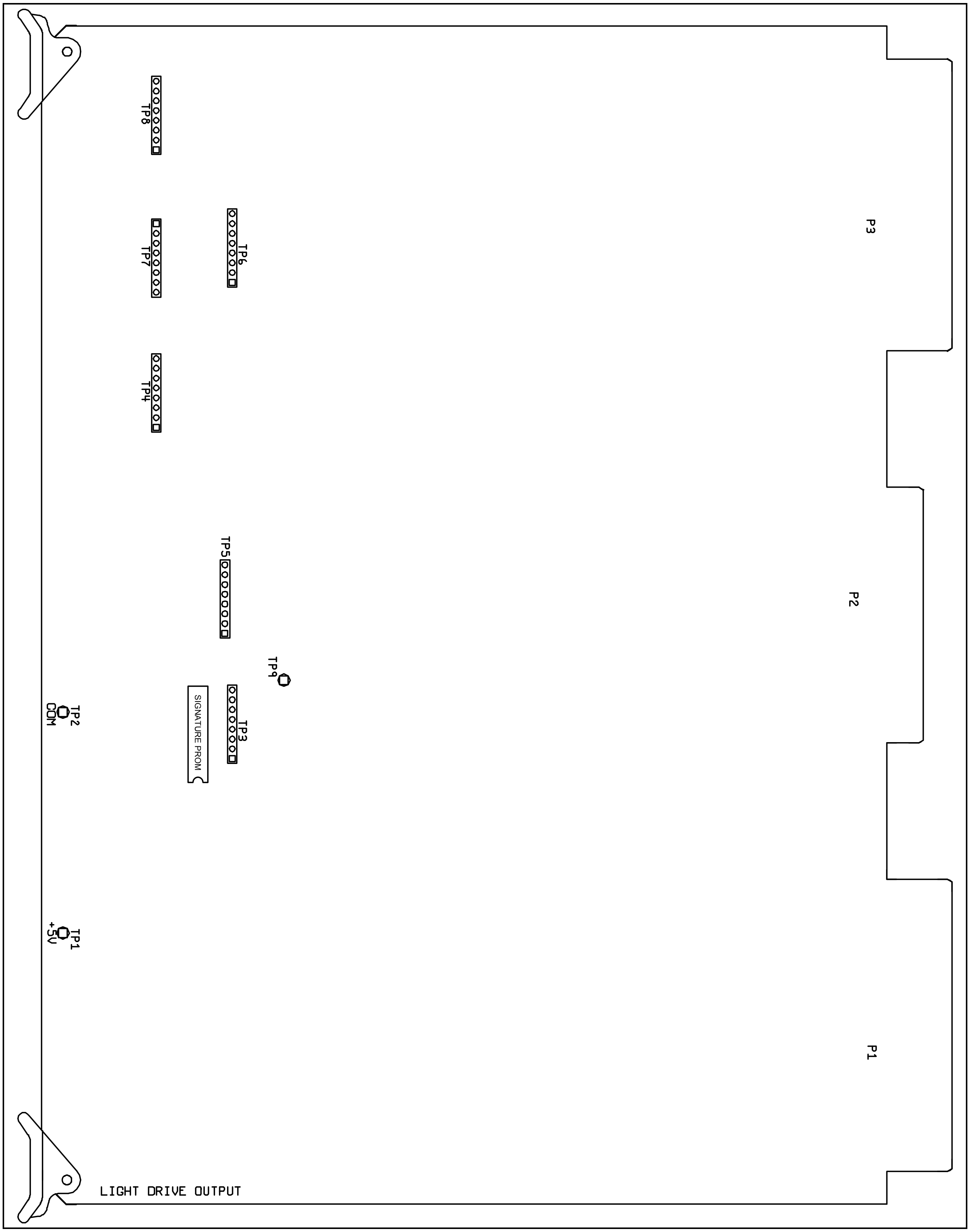

Figure 8–13. LDO Board Test Point and Signature PROM Locations

8.7.2. Card Edge Connectors

The LDO Board has three card edge connectors.

- P3, the top connector, is a 36-pin connector for Channels 1 through 4
  - See Table 8–13 for 36-pin configuration details
- P2, the middle connector, is a 50-pin connector that carries power, address and Vital I/O data; this connector is not user configurable
  - P2-35, P2-36, P2-40, P2-42, P2-43 and P2-44 through P2-48 are wired in a specific pattern per the application .lvc CAAPE report for board addressing; the remaining P2 pins are not user configurable
- P1, the lower connector, is a 36-pin connector for Channels 5 through 8
  - See Table 8–14 for 36-pin configuration details

Table 8–13. LDO Board 36-pin P3 Connections

P3-	Name	Function
1	OUTV1COM	Vital Power Common
2	+OUT4	Output 4
3 - 8		(not used)
9	OUTV1COM	Vital Power Common
10	+OUT3	Output 3
11 - 20		(not used)
21	OUTV1COM	Vital Power Common
22	+OUT2	Output 2
23		(not used)
24		(not used)
25	OUTV1COM	Vital Power Common
26	+OUT1	Output 1
27 - 32		(not used)
33	OUTV1COM	Vital Power Common
34	+V1OUT	Vital Power V+
35		(not used)
36		(not used)

Table 8–14. LDO Board 36-pin P1 Connections

P1-	Name	Function
1	OUTV2COM	Vital Power Common
2	+OUT8	Output 8
3 - 8		(not used)
9	OUTV2COM	Vital Power Common
10	+OUT7	Output 7
11 - 20		(not used)
21	OUTV2COM	Vital Power Common
22	+OUT6	Output 6
23		(not used)
24		(not used)
25	OUTV2COM	Vital Power Common
26	+OUT5	Output 5
27 - 32		(not used)
33	OUTV2COM	Vital Power Common
34	+V2OUT	Vital Power V+
35		(not used)
36		(not used)

8.7.3. Specifications/Assembly Differences

Table 8–15. LDO Board Specifications/Assembly Differences

Specification	59473-749		
	-02	-03	-04
Maximum Number of Output Boards Per VPI System	40		
Board Slots Required	1		
Number of Ports Per Board	8		
Maximum Board Logic Current Supply	500 mA		
Minimum Switched Output Supply Voltage (Vin)	9.0 VDC	15.0 VDC	9.0 VDC
Maximum Switched Output Supply Voltage (Vin)	18.0 VDC	30.0 VDC	18.0 VDC
Maximum Output Current Per Port (Iout)	2.9 A	2.9 A	2.9 A
Maximum Switched Power Per Port	52.2 W	87 W	52.2 W
Typical Output Voltage Drop	1.7 VDC	1.7 VDC	1.7 VDC
AOCD Current Threshold	65mA max	65mA max	65mA max
Isolation Between Outputs and 5 Volt Logic	> 3000 Vrms	> 3000 Vrms	> 3000 Vrms
Hot/Cold Filament Check	Yes, 100 mA	Yes, 200 mA	No *
Address Signature PROM Required	Yes	Yes	Yes

* Hot check only

WARNING

THE LDO BOARD MAY FAIL WITH UP TO 65 MILLIAMPERES OF OUTPUT LEAKAGE CURRENT WITH THE SYSTEM REQUESTING THE OUTPUT TO BE IN THE DE-ENERGIZED STATE. TO PREVENT A POTENTIAL UNSAFE CONDITION, ANY LOAD DEVICE ATTACHED TO A HIGH CURRENT VITAL OUTPUT CIRCUIT BOARD MUST NOT OPERATE AND MUST DE-ACTIVATE ABOVE 65 MILLIAMPERES. THIS INCLUDES ALL ENVIRONMENTAL OPERATING CONDITIONS AND ALL OPERATING VALUES OF THE LOAD DEVICE OVER ITS SERVICE LIFE. FAILURE TO FOLLOW THIS REQUIREMENT MAY LEAD TO UNEXPECTED OPERATION OF THE LOAD DEVICE.

8.8. LDO2 DETAILS

The lamp drive output 2 circuit handles high current to light signal lamps. Each output circuit can accommodate hot and cold filament checks. This output uses a FET switch in the common or return line of the circuit. Figure 8–14 shows the board interface.

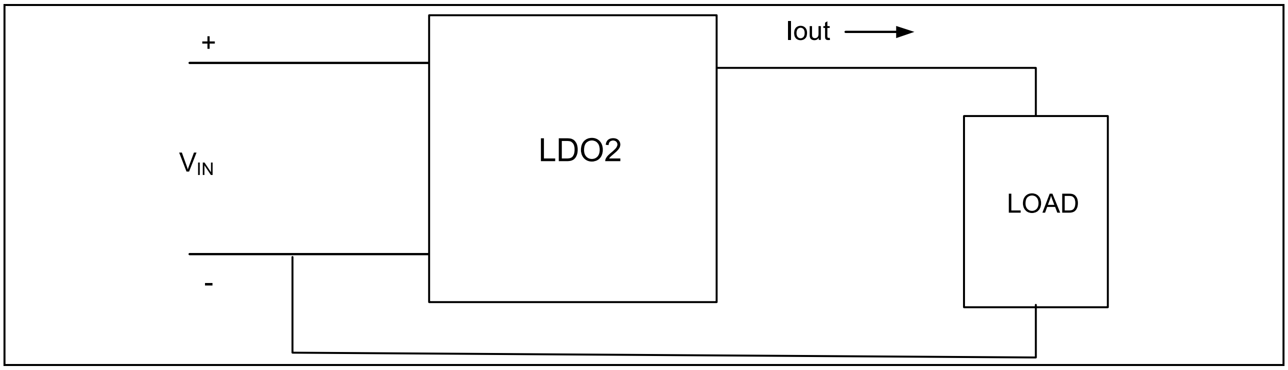

Figure 8–14. LDO2 Board Port Interface

In addition to the LDO board features, the LDO2 board has the following features:

- A Cable Integrity Check that uses isolated voltage sensing at the output to determine if a potential exists across the output when the output is off. A separate switch for each output can be used to select the system reaction to this event (log the error or drop the VPI II Vital Relay).

  Switch S4 switches 1-8 correspond to outputs 1-8 respectively. Enable position drops VRD if an external potential exists. Disable position does not drop VRD if an external potential exists.

- A Diagnostic Interface to VPI II CPU II board that registers all current readings and error conditions and can be read or cleared via the CPU II board.

- A Board Edge User Interface that registers all current readings and error conditions and can be read or cleared via a Board Edge User interface.

- A Current Monitor that reads the current through the output approximately every 200 milliseconds. This current can be compared to one of 8 different threshold levels (0.0, 0.55, 0.75, 0.95, 1.25, 1.55, 2.05, or 3.25 Amps) to turn the output off if it is not drawing the minimum required current. The use of the VPI II filament checking routines enables downgrading and prevents upgrading to signals that are not drawing the required current. The outputs are also guarded against overcurrent and short protection.

NOTE

The Current Monitor is not provided on P/N 31166-340-02.

8.8.1. LDO2 Board Test Points

TP1 though TP42 and TP44 are located on the front side of the board, while TP43 and TP45 through TP78 are located on the back side of the board. See Figure 8–15 for LDO2 board test points located on the front of the board.

Table 8–16. LDO2 Board Test Points

Test Points	
TP3, TP39	+5V, power
TP5, TP36	-V1
TP7, TP13, TP27, TP40	COM, common
TP17	+V1
TP29	+V2
TP1, TP2, TP4, TP6, TP8 - TP12, TP14 - TP16, TP18 - TP26, TP28, TP30 - TP35, TP37, TP38, TP40 - TP78	used in factory test

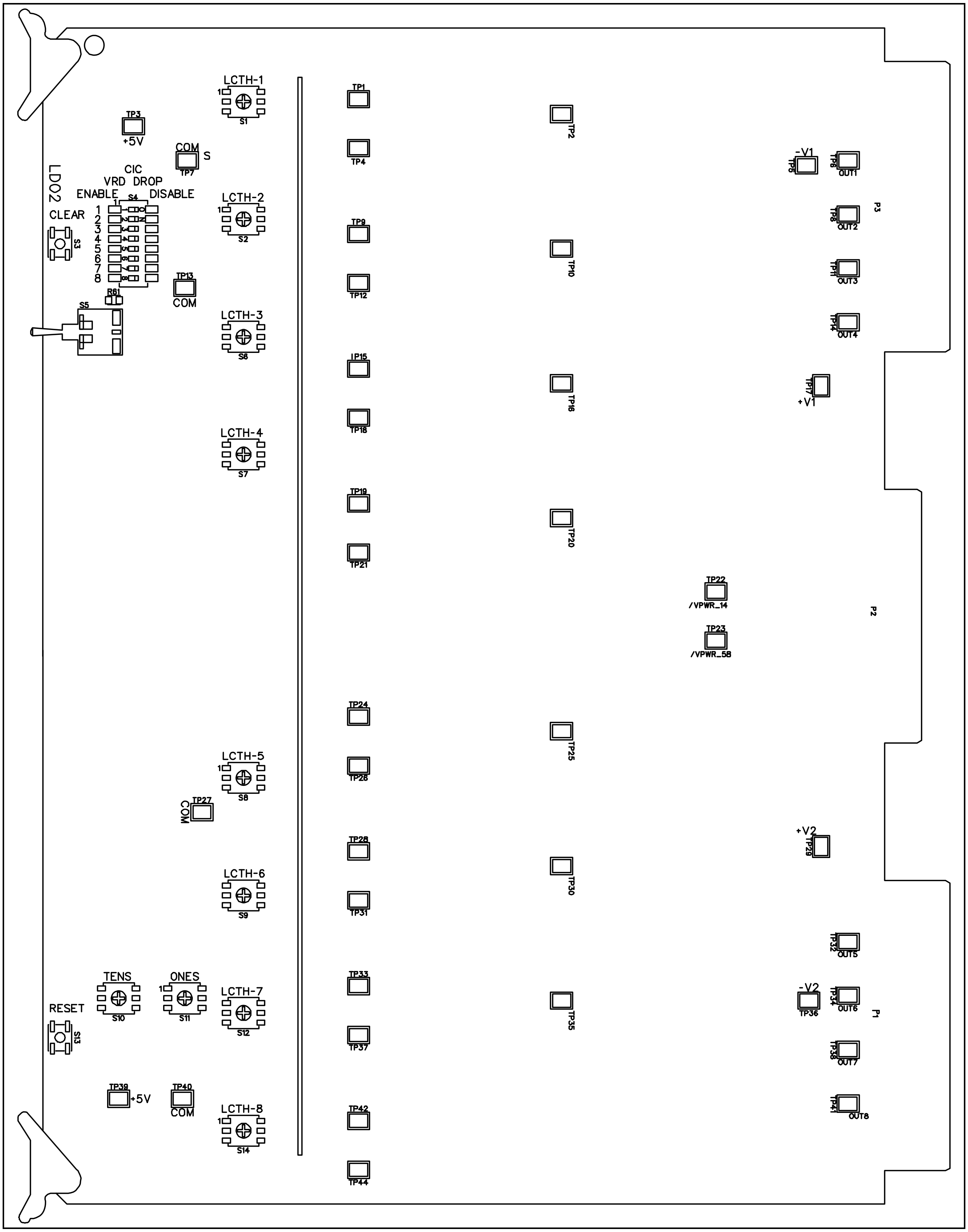

Figure 8–15. LDO2 Board Test Point and Switch Locations

8.8.2. LDO2 Board Switches

See Figure 8–15 for LDO2 board switch locations.

Table 8–17. LDO2 Board Switches

Switches	
S1	LCTH-1
S2	LCTH-2
S3	Clear
S4	CIC VRD Drop
S5	Toggle Switch
S6	LCTH-3
S7	LCTH-4
S8	LCTH-5
S9	LCTH-6
S10	Tens
S11	Ones
S12	LCTH-7
S13	Reset
S14	LCTH-8

Switches 1, 2, 6, 7, 8, 9, 12, and 14 are use to select the Low Current Threshold (LCTH). LCTH Switch locations are shown in Figure 8–15; an example selection dial is shown in Figure 8–16. Table 8–18 summarizes the switch settings.

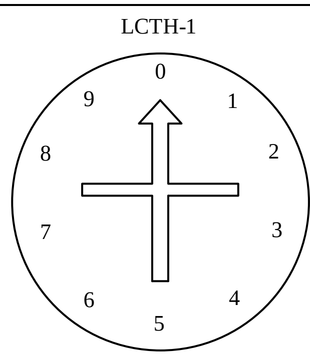

Figure 8–16. LCTH Selection Dial

Table 8–18. LCTH Switch Settings

Threshold	Switch Setting
0.0A	SW=0 Low Current Detection Disabled
0.55A	SW=1
0.75A	SW=2
0.95A	SW=3
1.25A	SW=4
1.55A	SW=5
2.05A	SW=6
3.25A	SW=7
0.0A	SW=8 Low Current Detection Disabled
0.55A	SW=9 (same as SW=1)

Switches 10 and 11 are used to select the appropriate AOCD PROM Group as specified by the compiled application (group 01 through 40). The switch locations are shown in Figure 8–15; selection dials are shown in Figure 8–17.

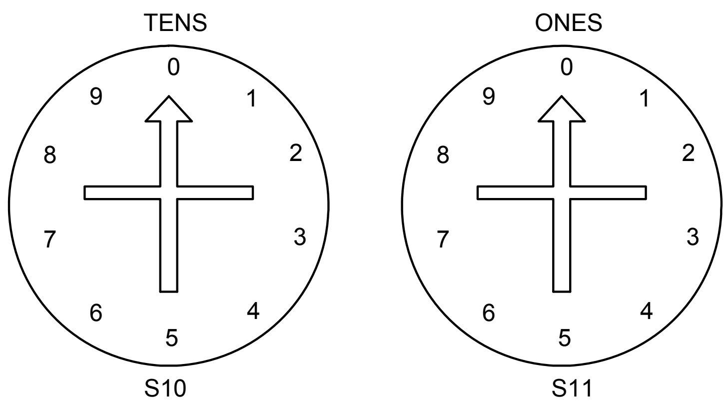

Figure 8–17. AOCD Selection Dials

8.8.3. Card Edge Connections

The LDO2 Board has three card edge connectors.

- P3, the top connector, is a 36-pin connector for Channels 1 through 4
  - See Table 8–19 for 36-pin configuration details
- P2, the middle connector, is a 50-pin connector that carries power, address and Vital I/O data
  - P2-35, P2-36, P2-40, P2-42, P2-43 and P2-44 through P2-48 are wired in a specific pattern per the application .lvc CAAPE report for board addressing; the remaining P2 pins are not user configurable
- P1, the lower connector, is a 36-pin connector for Channels 5 through 8
  - See Table 8–20 for 36-pin configuration details

Table 8–19. LDO2 Board 36-pin P3 Connections

P3-	Name	Function
1	+V1OUT	Vital Power V+
2	OUT4	Output 4+
3 - 8		(not used)
9	+V1OUT	Vital Power V+
10	OUT3	Output 3+
11 - 20		(not used)
21	+V1OUT	Vital Power V+
22	OUT2	Output 2+
23		(not used)
24		(not used)
25	+V1OUT	Vital Power V+
26	OUT1	Output 1+
27 - 32		(not used)
33	-V1OUT	Vital Power Common
34	+V1OUT	Vital Power V+
35		(not used)
36		(not used)

Table 8–20. LDO2 Board 36-pin P1 Connections

P1-	Name	Function
1	+V2OUT	Vital Power V+
2	OUT8	Output 8+
3 - 8		(not used)
9	+V2OUT	Vital Power V+
10	OUT7	Output 7+
11 - 20		(not used)
21	+V2OUT	Vital Power V+
22	OUT6	Output 6+
23		(not used)
24		(not used)
25	+V2OUT	Vital Power V+
26	OUT5	Output 5+
27 - 32		(not used)
33	-V2OUT	Vital Power Common
34	+V2OUT	Vital Power V+
35		(not used)
36		(not used)

8.8.4. Specifications/Assembly Differences

Table 8–21. LDO2 Board Specifications/Assembly Differences

Specification	31166-340	
	-01	**-02**
Maximum Number of Output Boards Per VPI System	40	
Board Slots Required	1	
Number of Ports Per Board	8	
Maximum Board Logic Current Supply	350 mA	250 mA
Minimum Switched Output Supply Voltage (Vin)	9.0 VDC	
Maximum Switched Output Supply Voltage (Vin)	18.0 VDC	
Maximum Output Current Per Port (Iout)	3.3 A	
Maximum Output Current Per 4-Port Group	7.5 A	
Typical Output Voltage Drop	1.0 VDC	
Cable Integrity Check Detection Voltage	3.0 ± 0.3 V	
Over Current Shutdown Threshold (t = 200 to 400 ms)	4.0 A	none
Low Level Current Detection Threshold Range	0.55 to 3.25 A in 7 steps	none
AOCD Current Threshold	65mA max	
Isolation Between Outputs and 5 Volt Logic	> 3000 Vrms	
Hot/Cold Filament Check	Yes, 100 mA	Yes, 100 mA
Address Signature PROM Required	No	

WARNING

THE LDO BOARD MAY FAIL WITH UP TO 65 MILLIAMPERES OF OUTPUT LEAKAGE CURRENT WITH THE SYSTEM REQUESTING THE OUTPUT TO BE IN THE DE-ENERGIZED STATE. TO PREVENT A POTENTIAL UNSAFE CONDITION, ANY LOAD DEVICE ATTACHED TO A HIGH CURRENT VITAL OUTPUT CIRCUIT BOARD MUST NOT OPERATE AND MUST DE-ACTIVATE ABOVE 65 MILLIAMPERES. THIS INCLUDES ALL ENVIRONMENTAL OPERATING CONDITIONS AND ALL OPERATING VALUES OF THE LOAD DEVICE OVER ITS SERVICE LIFE. FAILURE TO FOLLOW THIS REQUIREMENT MAY LEAD TO UNEXPECTED OPERATION OF THE LOAD DEVICE.

9. SECTION 9 – ACO (AC OUTPUT) BOARD, P/N 59473-937-XX

9.1. INTRODUCTION

This section provides Vital ACO board detail.

9.2. GENERAL

The Vital AC Output (ACO) board operates in a manner similar to Vital Output boards. It is used for lighting signal lamps or for operating other AC loads requiring less than 0.8 ampere. The board has 8 outputs divided into two groups of four. Outputs 1 through 4 are connected to one power supply input while outputs 5 through 8 are connected to a second power supply input. In Vital applications, these power supply inputs are connected to a source that can be vitally turned off (usually a contact of the VPI Vital relay or one of its repeaters).

9.3. OPERATION

The ACO board has three main modes of operation: READ, WRITE and CIRCULATE:

- READ MODE: in the read mode, the data from the RAM is read. Since data is stored vertically in the RAM, each group of 8-bits represents one bit of each of the 8 words. This data is serially clocked into shift registers on the I/O Bus Interface board. Each shift register receives one bit for each read operation. After 8 read operations, a particular shift register contains 8 of the 32-bits of a particular output checkword. The shift register data is then stored in CPU memory. This process continues until the entire 32-bit word is read and stored for all of the outputs.

- WRITE MODE: in the write mode, the RAM is filled with all “ones”.

- CIRCULATE MODE: In the circulate mode, the even or odd polynomial is selected depending on which recheck cycle is in process and the 32-bit words are cycled through the AOCD circuitry 11 times.

Figure 9–1 shows a block diagram of the Vital AC Output board. The outputs of this board are turned on by writing a ‘1’ to the output and turned off by writing a ‘0’. The main processing system controls the status of the outputs by setting the data bus lines to the data pattern corresponding to the desired output on/off status and writing that data to the output board. Because the system has a 16-bit wide data bus, 16 outputs can be updated at once. To do this, two output boards are given the same address and

- one board is connected to the lower half of the data bus

- the other is connected to the upper half

For the board on the lower half of the bus, output 1 corresponds to data bus line 0 and output 8 is data line 7. For the board on the upper half, output 1 is data line 8 and output 8 is data line F.

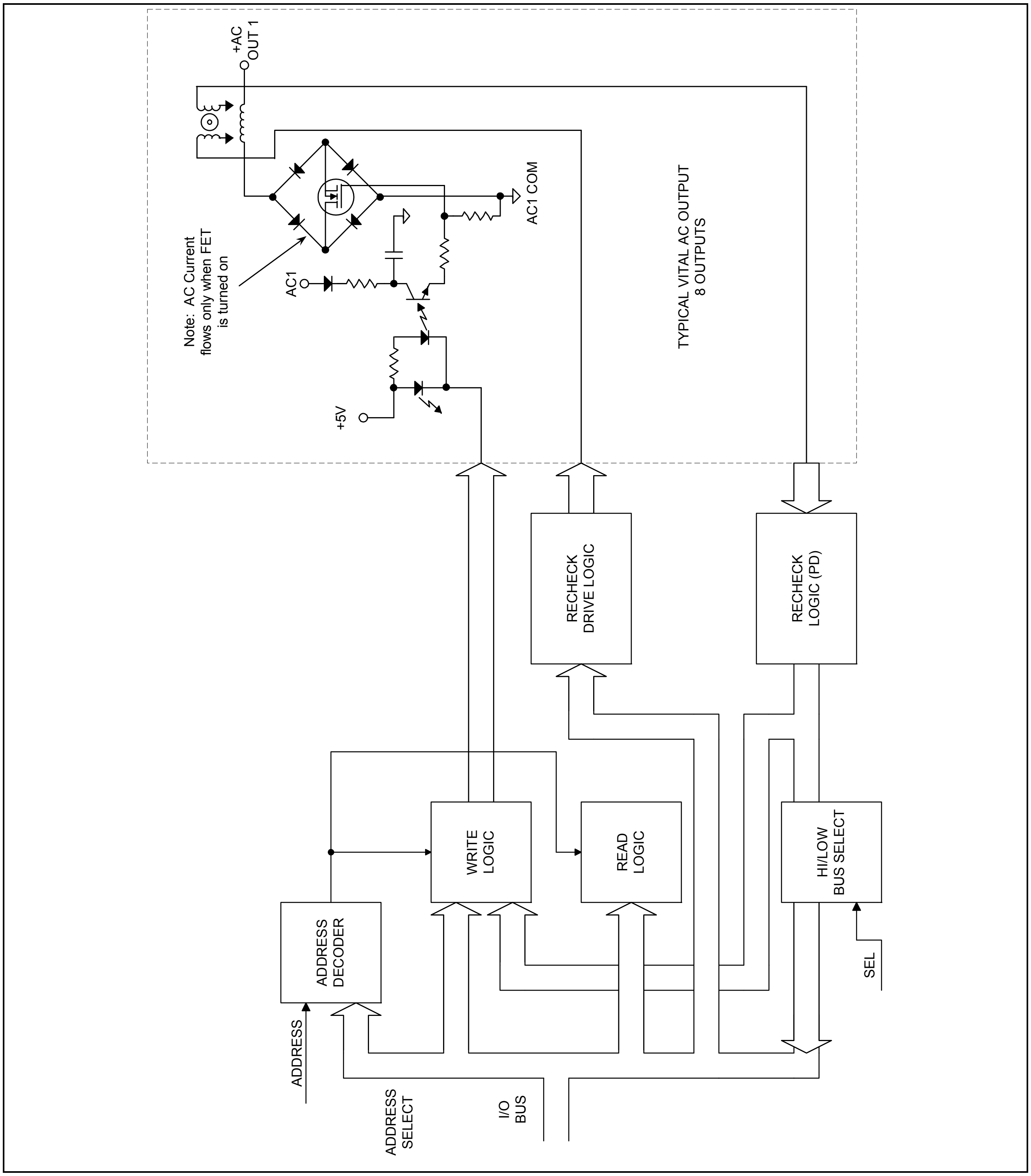

Figure 9–1. ACO Board Block Diagram

Besides turning the outputs on and off, the circuit must verify each output is in the correct state. To check the outputs, each individual output contains PROM-defined AOCD circuitry that monitors its output current flow. The AOCD PROM chip (see Appendix A for more information) is designated U12. The AOCD passes a digital signal if, and only if, the current in its output winding is less than a specified level. Each output board contains the necessary logic to circulate a digital word through the AOCD, read the resultant word at the output of the AOCD, divide it by a preset polynomial and store the result. Every 50 ms the main processing system reads the result of this process. If the output was supposed to be in its off state, the result indicates there was current flow less than 50 mA for the entire 50 ms period.

WARNING

VPI USERS MUST CONFIRM THAT OUTPUT DEVICE CURRENT REQUIREMENTS ARE CONSISTENT WITH AOCD CURRENT THRESHOLD CHARACTERISTICS.

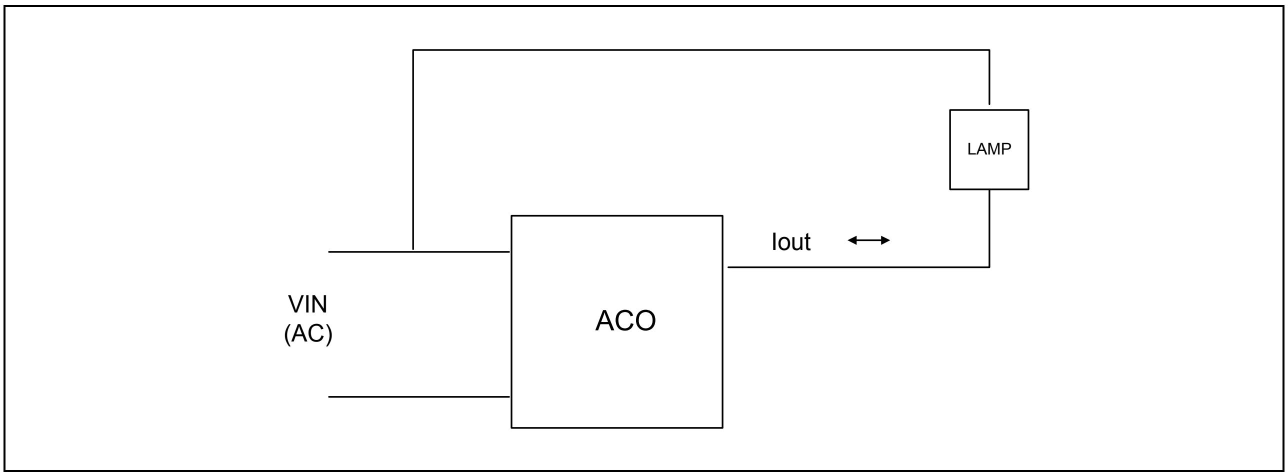

Figure 9–2. ACO Board Port Interface

9.4. INDICATIONS

Figure 9–3 shows the ACO board edge, including indications.

ACO BOARD
59473-937-XX

NORMAL INDICATION	PCB NOTATION	FUNCTION
FLASHING, MOSTLY OFF	CR1	RD (Recheck data Is Being Read From The Board)
FLASHING, MOSTLY OFF	CR2	WR (Output Ports Are Being Updated)
OFF, ON, FLASHING	CR3	CH1 (Output #1)
OFF, ON, FLASHING	CR4	Output #2
OFF, ON, FLASHING	CR5	Output #3
OFF, ON, FLASHING	CR6	Output #4
OFF, ON, FLASHING	CR7	Output #5
	E1	+5V (+5V Test Point)
OFF, ON, FLASHING	CR8	Output #6
OFF, ON, FLASHING	CR9	Output #7
	E2	5V COM (5V Common Test Point)
OFF, ON, FLASHING	CR10	CH8 (Output #8)

CR3 - CR10 Light when output is commanded to be on by the CPU.

Figure 9–3. ACO Board Edge

9.5. JUMPER CONFIGURATIONS

In the system module, the ACO board's address is established by wire wrapping selected terminals P2-44, P2-45, P2-46 and/or P2-47 to 5V common.

When a wire wrap jumper is installed between PC2-40 and PC2-42, the board in that slot is connected to the lower data bus. When the jumper is installed between PC2-40 and PC2-43, the board is connected to the upper data bus.

9.6. TRANSIENT PROTECTION

To prevent interference from transients and other local noise, this board contains EMI and MOV filters on the outputs and capacitive filters in the power supply circuitry. These filters are very effective in combating interference when combined with good earth grounding of the VPI system.

9.7. TEST POINTS

See Figure 9–4 for ACO board test point locations.

Table 9–1. ACO Board Test Points

Test Points	
E1	+5V, power
E2	COM, common

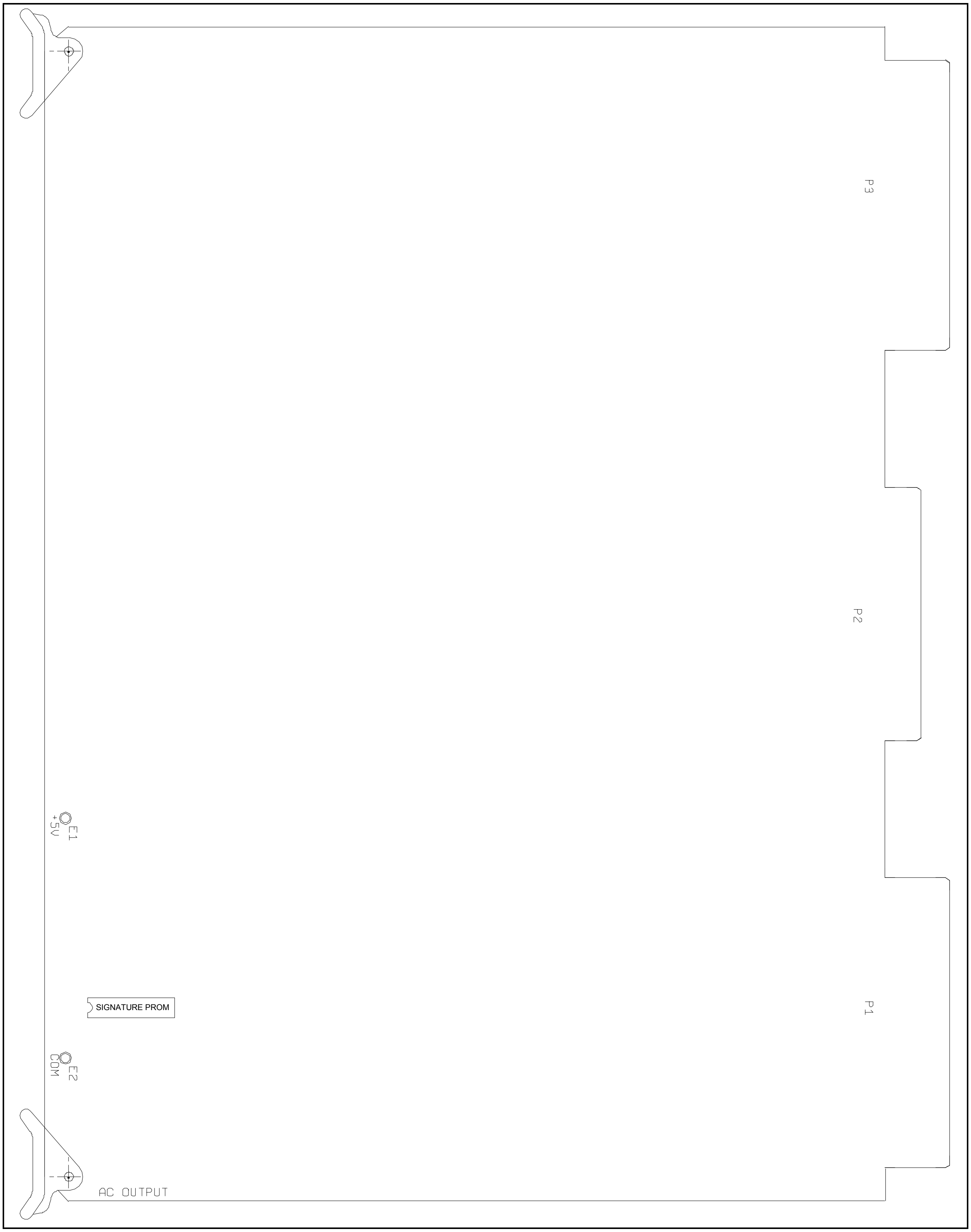

Figure 9–4. ACO Board Test Point and PROM Locations

9.8. CARD EDGE CONNECTORS

The ACO Board has three card edge connectors.

- P3, the top connector, is a 36-pin connector for Channels 1 through 4
  - See Table 9–2 for 36-pin configuration details
- P2, the middle connector, is a 50-pin connector that carries power, address and Vital I/O data
  - P2-42 or P2-43 are wired to P2-40 and P2-44 through P2-47 are wired in a specific pattern to common P2-48 per the application .lvc CAAPE report for board addressing; the remaining P2 pins are not user configurable
- P1, the lower connector, is a 36-pin connector for Channels 5 through 8
  - See Table 9–3 for 36-pin configuration details

Table 9–2. ACO Board 36-pin P3 Connections

P3-	Name	Function
1	OUTV1COM	Vital Power Common
2	+OUT4	Output 4
3 - 8		(not used)
9	OUTV1COM	Vital Power Common
10	+OUT3	Output 3
11 - 20		(not used)
21	OUTV1COM	Vital Power Common
22	+OUT2	Output 2
23		(not used)
24		(not used)
25	OUTV1COM	Vital Power Common
26	+OUT1	Output 1
27 - 32		(not used)
33	OUTV1COM	Vital Power Common
34	+V1OUT	Vital Power V+
35		(not used)
36		(not used)

Table 9–3. ACO Board 36-pin P1 Connections

P1-	Name	Function
1	OUTV2COM	Vital Power Common
2	+OUT8	Output 8
3 - 8		(not used)
9	OUTV2COM	Vital Power Common
10	+OUT7	Output 7
11 - 20		(not used)
21	OUTV2COM	Vital Power Common
22	+OUT6	Output 6
23		(not used)
24		(not used)
25	OUTV2COM	Vital Power Common
26	+OUT5	Output 5
27 - 32		(not used)
33	OUTV2COM	Vital Power Common
34	+V2OUT	Vital Power V+
35		(not used)
36		(not used)

9.9. SPECIFICATIONS

WARNING

LOW CURRENT VITAL AC OUTPUT BOARDS MAY FAIL WITH UP TO 3 MILLIAMPERES OF OUTPUT LEAKAGE CURRENT WITH THE SYSTEM REQUESTING THE OUTPUT TO BE IN THE DE-ENERGIZED STATE. TO PREVENT A POTENTIAL UNSAFE CONDITION, ANY LOAD DEVICE ATTACHED TO A LOW CURRENT VITAL OUTPUT CIRCUIT BOARD MUST NOT OPERATE AND MUST DE-ACTIVATE ABOVE 3 MILLIAMPERES. THIS INCLUDES ALL ENVIRONMENTAL OPERATING CONDITIONS AND ALL OPERATING VALUES OF THE LOAD DEVICE OVER ITS SERVICE LIFE. FAILURE TO FOLLOW THIS REQUIREMENT MAY LEAD TO UNEXPECTED OPERATION OF THE LOAD DEVICE.

WARNING

HIGH CURRENT VITAL AC OUTPUT BOARDS MAY FAIL WITH UP TO 65 MILLIAMPERES OF OUTPUT LEAKAGE CURRENT WITH THE SYSTEM REQUESTING THE OUTPUT TO BE IN THE DE-ENERGIZED STATE. TO PREVENT A POTENTIAL UNSAFE CONDITION, ANY LOAD DEVICE ATTACHED TO A HIGH CURRENT VITAL OUTPUT CIRCUIT BOARD MUST NOT OPERATE AND MUST DE-ACTIVATE ABOVE 65 MILLIAMPERES. THIS INCLUDES ALL ENVIRONMENTAL OPERATING CONDITIONS AND ALL OPERATING VALUES OF THE LOAD DEVICE OVER ITS SERVICE LIFE. FAILURE TO FOLLOW THIS REQUIREMENT MAY LEAD TO UNEXPECTED OPERATION OF THE LOAD DEVICE.

Table 9–4. ACO Board Specifications/Assembly Differences

Specification	59473-937 -02	59473-937 -03
Maximum Number of Boards Per VPI System	40	
Board Slots Required	1	
Number of Ports Per Board	8	
Maximum Board Logic Current Supply	500mA	
Minimum Switched Output Supply Voltage	90 VAC	90 VAC
Maximum Switched Output Supply Voltage	130 VAC	130 VAC
Frequency Range	40 - 150 Hz	40 - 150 Hz
AOCD Operating Threshold	65 mA max	3 mA max
Maximum Output Current Per Port	0.8 A rms	0.5 A rms
Switched Power (max resistive)	104 W	104 W
Isolation Between Outputs	> 3000 Vrms	> 3000 Vrms
Special EMI Suppression	No	Yes
Address Signature PROM Required	Yes	Yes

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10. SECTION 10 – FSVT (FIELD-SETTABLE VITAL TIMER) BOARD, P/N 59473-894-XX

10.1. INTRODUCTION

This section provides FSVT board detail.

10.2. GENERAL

The Field Settable Vital Timer (FSVT) board is located on the Vital I/O bus. It is used to provide Vital timing functions that can be changed without recompiling the application data.

10.3. OPERATION

Normal operation of the FSVT board includes detecting the timer's setting and then performing a Vital algorithm to verify the setting of that timer's switch is accurate.

The FSVT board contains provisions for the use of 8 field-settable Vital timing functions. Time setting selection is accomplished through the programming of the time selection jumpers. Each of the 8 timers has four pin headers that allow setting of the desired time interval by positioning one jumper in each header. Time is specified in tens of minutes, units of minutes, tens of seconds and units of seconds. The correct times settings are typically included in a location's Book of Plans. A label on the board provides a means of listing the timer settings.

CAUTION

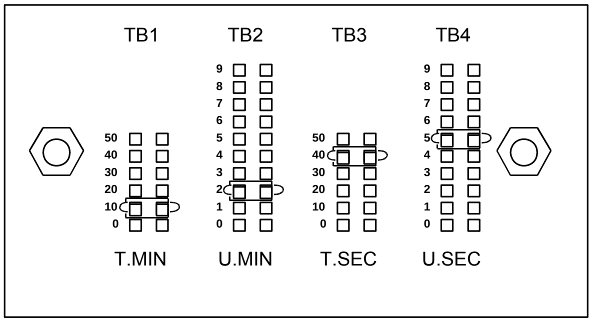
> Failure to install all four jumpers for a timer or installing more than one on a header results in an infinite timing cycle, so the timer never times out.

Figure 10–1 shows two examples of FSVT board timer setting examples. See Figure 10–4 for the timer locations.

SET FOR
12 MINUTES, 45 SECONDS

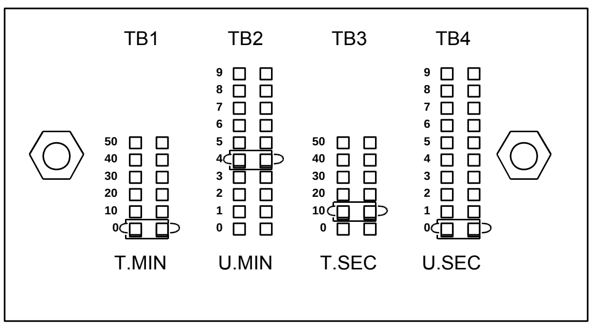
ONE JUMPER MUST BE INSTALLED IN EACH COLUMN

JUMPER ORIENTATION:



(0 to 59 Min. & 59 Sec.)

SET FOR
4 MINUTES, 10 SECONDS



(0 to 59 Min. & 59 Sec.)

Figure 10–1. FSVT Board Timer Setting Examples

On the board front edge are LED indicators showing which of the 8 timing functions are active. In addition, test points useful in troubleshooting internal operation are available at the board front edge. Figure 10–2 shows the FSVT board edge, including indicators.

Once the Vital timers have been programmed by installing the jumpers, the settings can be "sealed" under a clear plastic cover using sealing wire and plastic seals. The kit also contains an extra label for recording new timer settings. The label contains a pressure sensitive adhesive so it can be applied over the existing label. Extra sealing kits can be obtained by ordering Alstom P/N 59649-219-01.

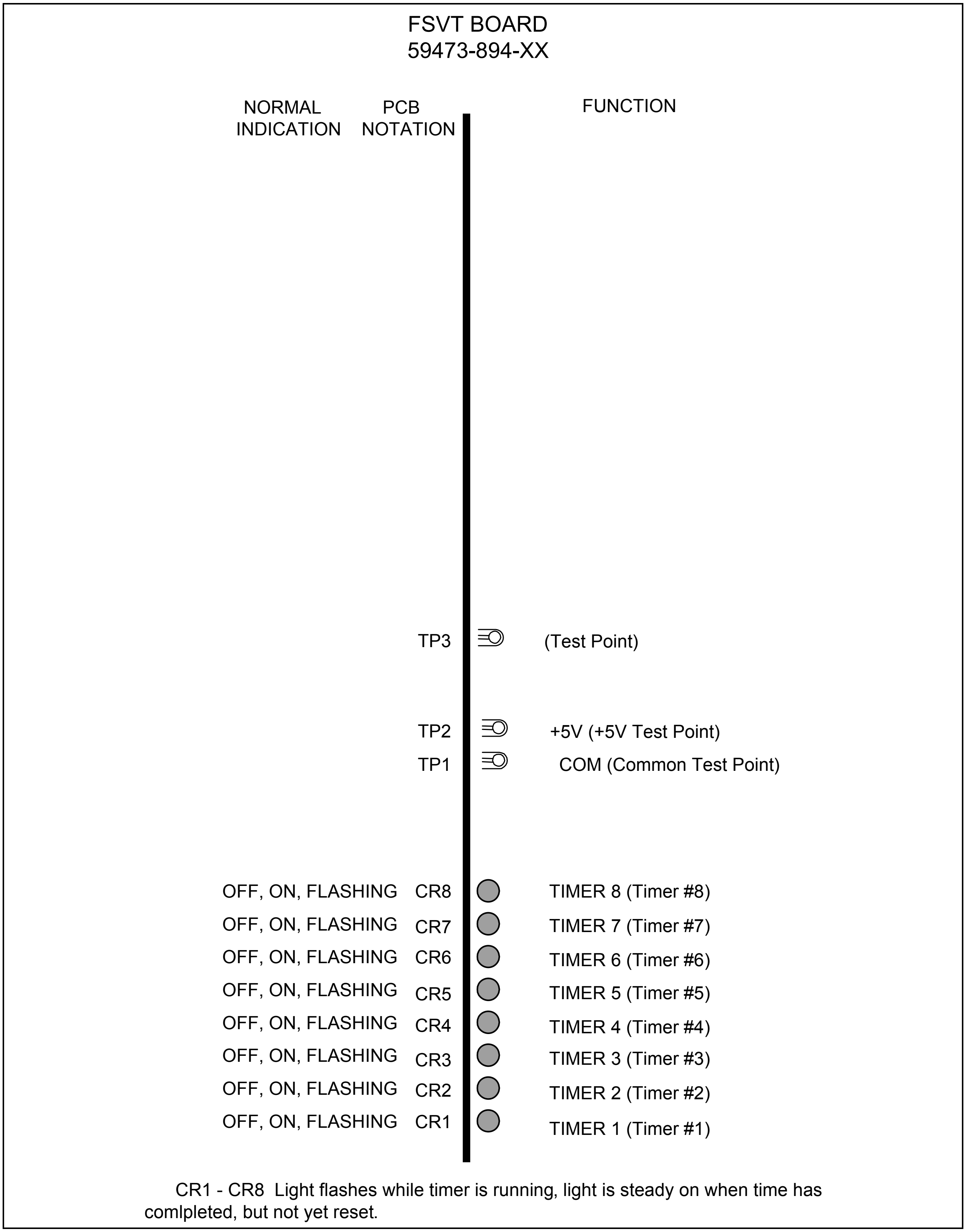


Figure 10–2. FSVT Board Edge

10.4. TEST POINTS

Table 10–1 lists the FSVT board test points and Figure 10–3 shows the test point locations.

Table 10–1. FSVT Board Test Points

Test Points	
TP1	COM, common
TP2	+5V, power
TP3	used for factory test
PC1	used for factory test

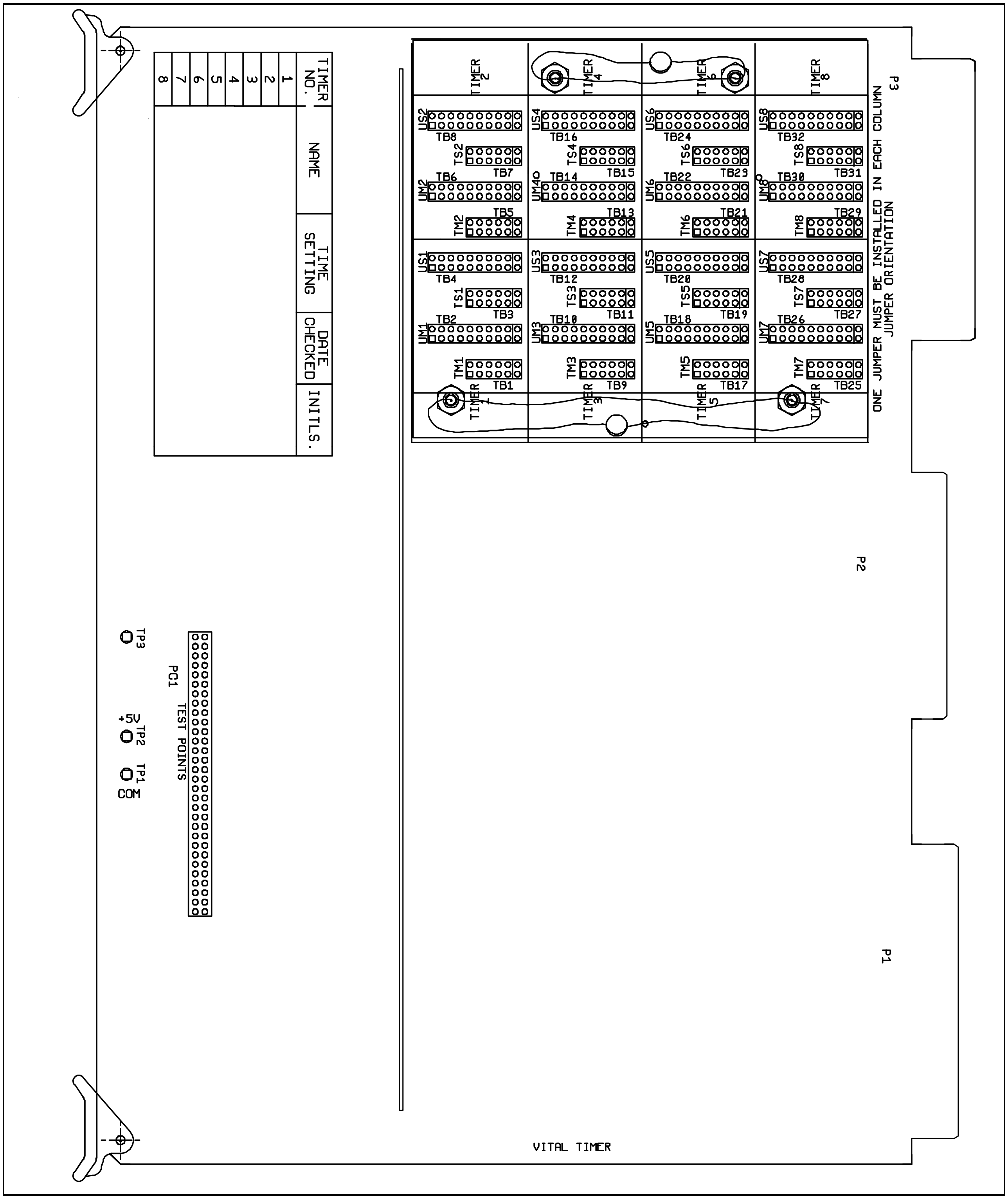


Figure 10–3. FSVT Board Test Point and Timer Locations

10.5. CARD EDGE CONNECTORS

The FSVT Board has three card edge connectors.

- P3, the top connector, is a 36-pin connector used only for mechanical board retention; this connector is not user configurable
- P2, the middle connector, is a 50-pin connector that carries power, address and Vital I/O data
  - P 2-44 through P2-47 are wired in a specific pattern to common P2-48 per the application .lvc CAAPE report for board addressing; the remaining P2 pins are not user configurable
- P1, the lower connector, is a 60-pin connector used only for mechanical board retention; this connector is not user configurable

10.6. SPECIFICATIONS

Table 10–2. FSVT Board Specifications/Assembly Differences:

Specification	**59473-894**	
	-01	**-02**
Maximum Number of Boards Per VPI System	2 (1 of each type)	
Board Slots Required	1	
Logic Voltage Range	4.75 to 5.25 Volts	
Logic Current Load (Maximum)	500 mA	
Number of Discrete Timers Per Board	8	
Used for Vital Timers Number	1 through 8	9 through 16
Minimum Run Time (minutes/seconds)	0:00	
Maximum Run Time (minutes/seconds)	59:59	
Assign to I/O Bus With Signature Header Drawing No. (ID letter)	59473-871-01 (A)	
Jumper TB4 Timer Settings (min/max)	00/09 seconds	
Jumper TB3 Timer Settings (min/max)	0/50 seconds	
Jumper TB2 Timer Settings (min/max)	00/09 minutes	
Jumper TB1 Timer Settings (min/max)	0/50 minutes	
Time Setting Method	Jumper Selection	

A. APPENDIX A – SIGNATURE HEADERS AND PROMS

A.1. INTRODUCTION

This appendix provides VPI circuit boards Signature Header and PROM information.

A.2. GENERAL

This section provides VPI circuit boards Signature Header and PROM information. Address Signature Headers (for Vital inputs and I/O Bus boards) have assigned signature letters, summarized in Table A–1.

Table A–1. Address Signature Headers (For Vital Inputs and I/O Bus Boards)

Address Signature Header Drawing Number	Address Signature Letter
59473-871-01	A
59473-871-02	B
59473-871-03	C
59473-871-04	D
59473-871-05	E
59473-871-06	F
59473-871-07	G
59473-871-08	H
59473-871-09	I
59473-871-10	J
59473-871-11	K
59473-871-12	L
59473-871-13	M
59473-871-14	N
59473-871-15	O
59473-871-16	P

Address Signature PROMs for all Vital output boards except LDO2 are provided in Table A–2.

Table A–2. Address Signature PROMs

Signature Number (Vital Output Board Number)	Signature PROM Drawing Number	Selectable Signature PROM Switch Settings		Signature Number (Vital Output Board Number)	Signature PROM Drawing Number	Selectable Signature PROM Switch Settings	
		tens	ones			tens	ones
1	39780-003-01	0	1	21	39780-003-21	2	1
2	39780-003-02	0	2	22	39780-003-22	2	2
3	39780-003-03	0	3	23	39780-003-23	2	3
4	39780-003-04	0	4	24	39780-003-24	2	4
5	39780-003-05	0	5	25	39780-003-25	2	5
6	39780-003-06	0	6	26	39780-003-26	2	6
7	39780-003-07	0	7	27	39780-003-27	2	7
8	39780-003-08	0	8	28	39780-003-28	2	8
9	39780-003-09	0	9	29	39780-003-29	2	9
10	39780-003-10	1	0	30	39780-003-30	3	0
11	39780-003-11	1	1	31	39780-003-31	3	1
12	39780-003-12	1	2	32	39780-003-32	3	2
13	39780-003-13	1	3	33	39780-003-33	3	3
14	39780-003-14	1	4	34	39780-003-34	3	4
15	39780-003-15	1	5	35	39780-003-35	3	5
16	39780-003-16	1	6	36	39780-003-36	3	6
17	39780-003-17	1	7	37	39780-003-37	3	7
18	39780-003-18	1	8	38	39780-003-38	3	8
19	39780-003-19	1	9	39	39780-003-39	3	9
20	39780-003-20	2	0	40	39780-003-40	4	0

Figure A–1 shows the Selectable Signature PROM assembly. The locations of key reference points are indicated to assist in installing and configuring the device. The figure shows the selection of “01” to be installed on the first Vital output board of a system.

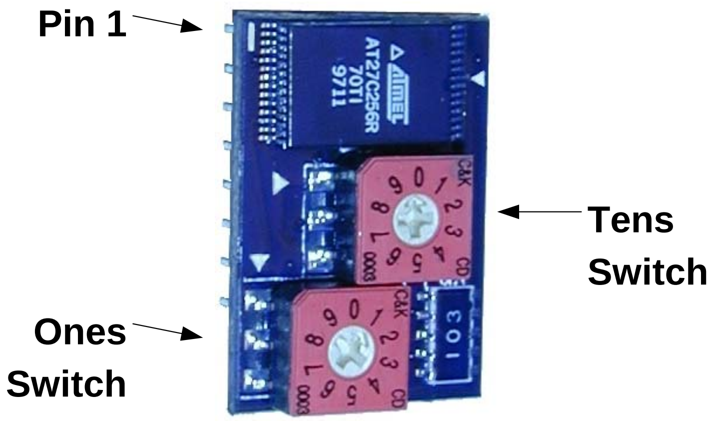


Figure A–1. Selectable Signature PROM Assembly

NOTE

This assembly is designed to replace a 16-pin integrated circuit that is installed in a Vital output board of a VPI system. The Alstom drawing numbers of these integrated circuits are listed in the table above under the heading “Signature PROM Drawing No.”

NOTE

The location and orientation of the 16-pin socket where this assembly is to be installed varies for the different board types. Be careful to observe the location of Pin 1 when installing this assembly.

NOTE

This assembly should be handled carefully as damage to the 16 machined pins may result. While the pins on this assembly are quite strong, they are made of a material that cannot be bent often without breaking.

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B. APPENDIX B – VITAL BOARD LAYOUT DRAWINGS

B.1. INTRODUCTION

This appendix provides the layout drawings for each Vital board type.

B.2. GENERAL

This appendix contains layout drawings of the boards discussed in this manual.

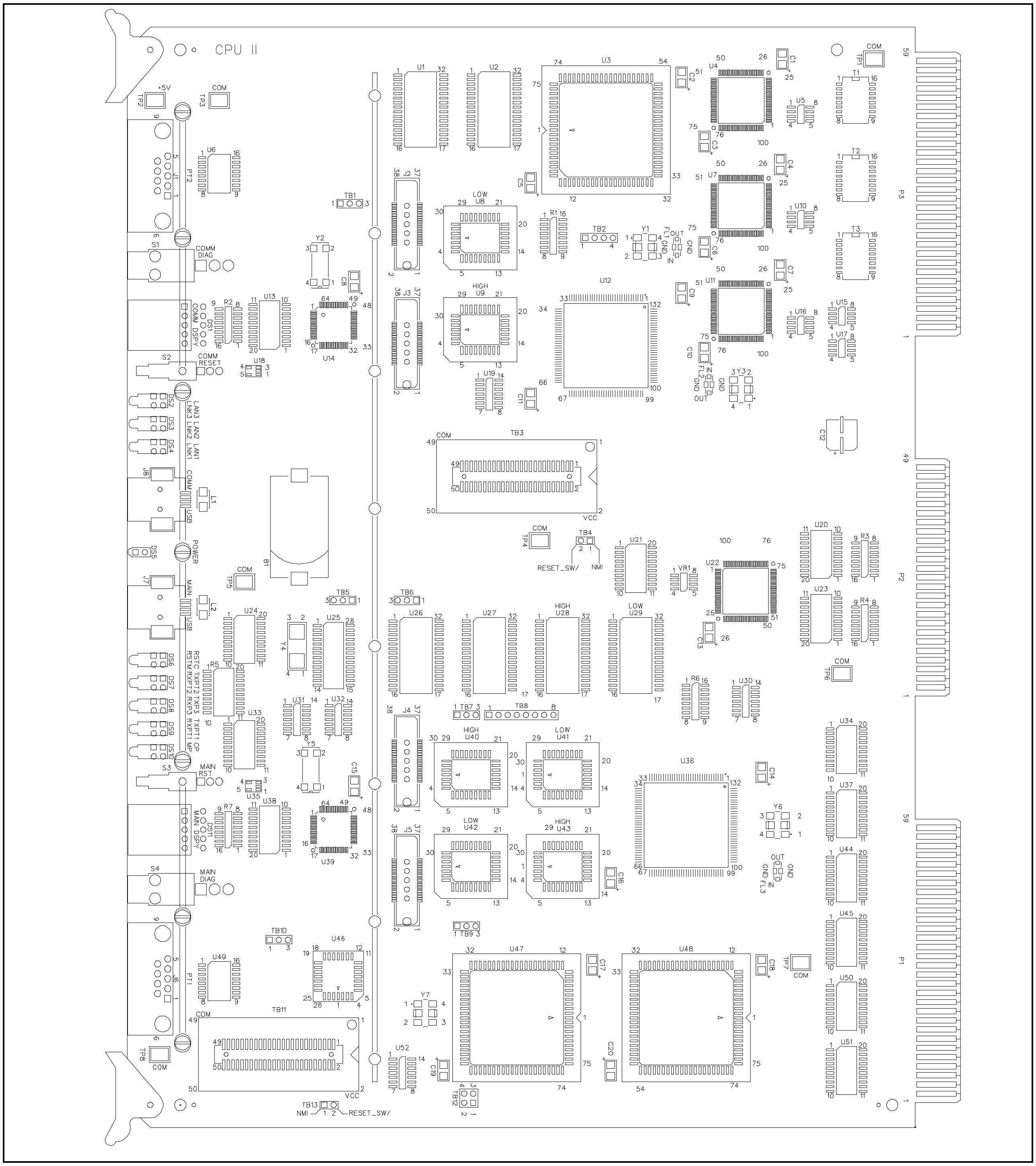

Figure B–1. CPU II Board, P/N 31166-374-00

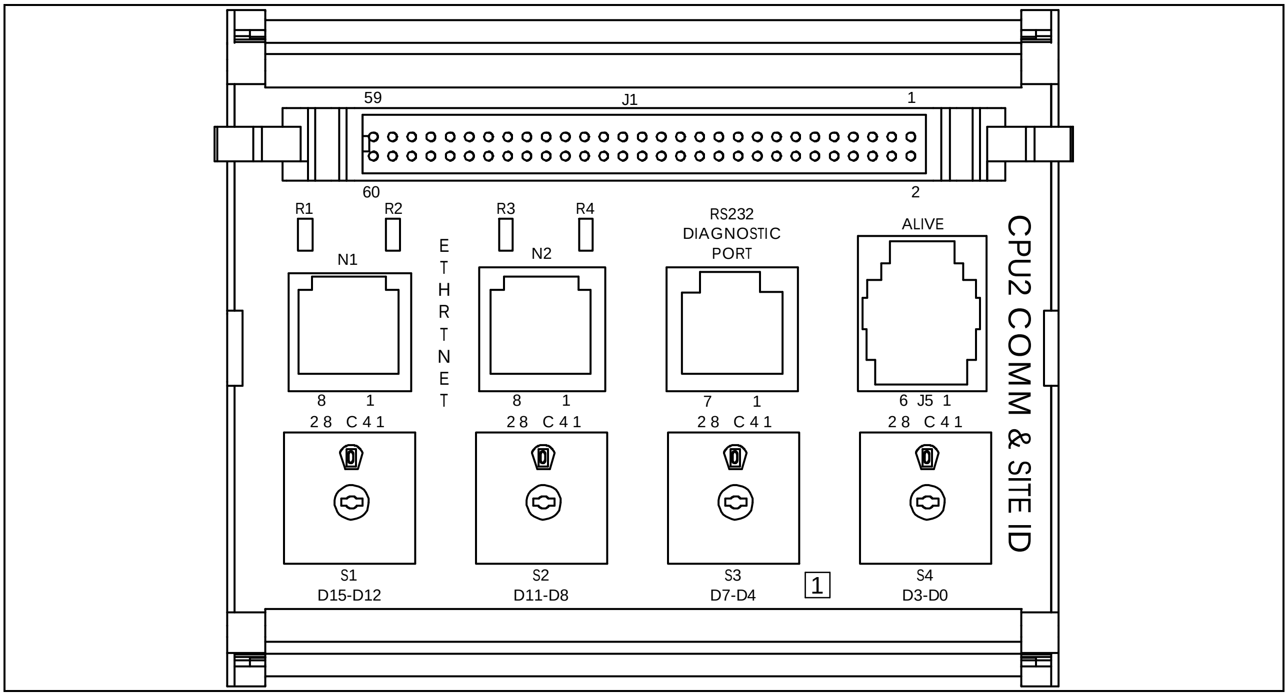

Figure B–2. CPU2 Interface Board, P/N 31166-499-00

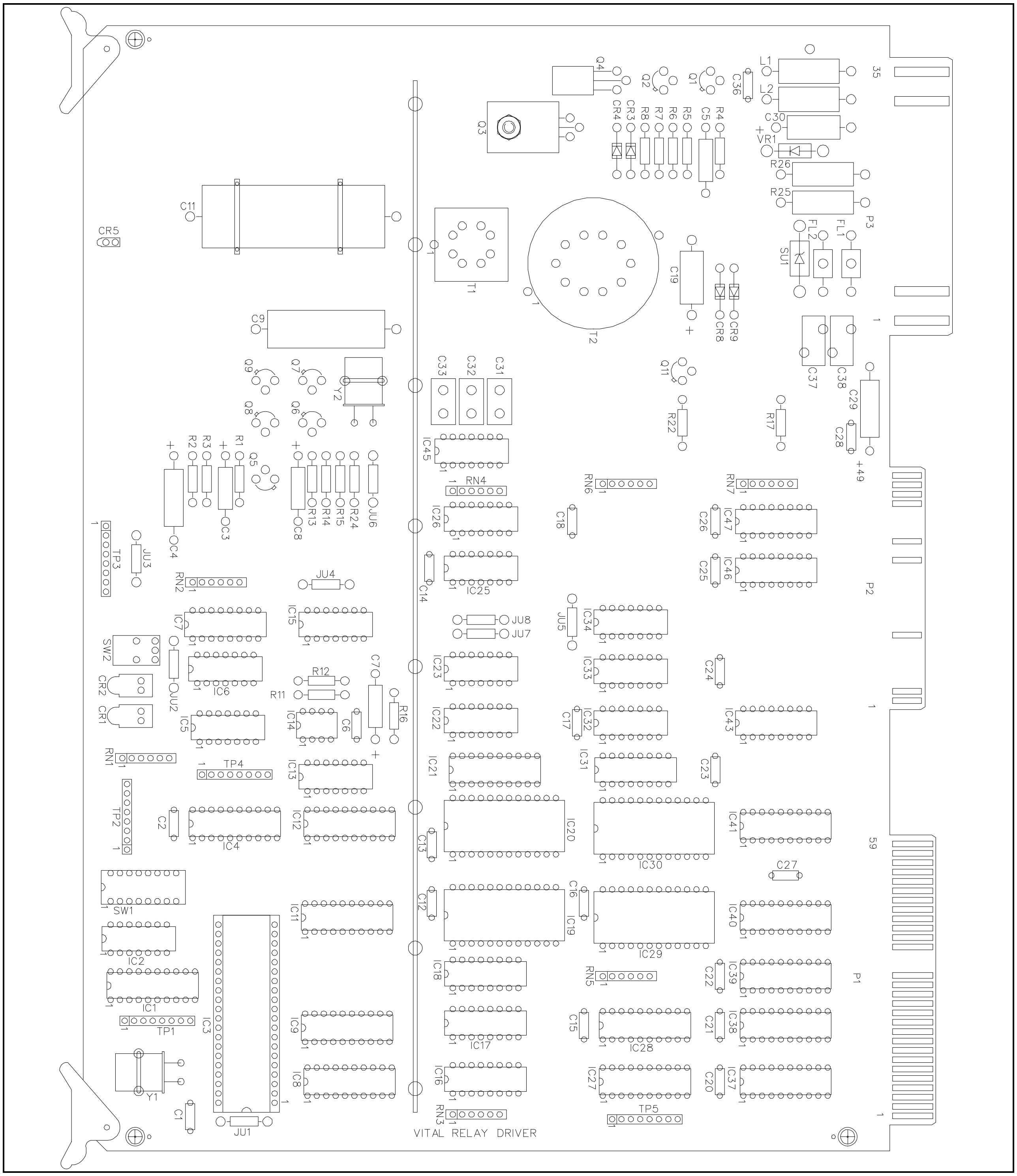

Figure B–3. VRD Board, P/N 59473-740-00

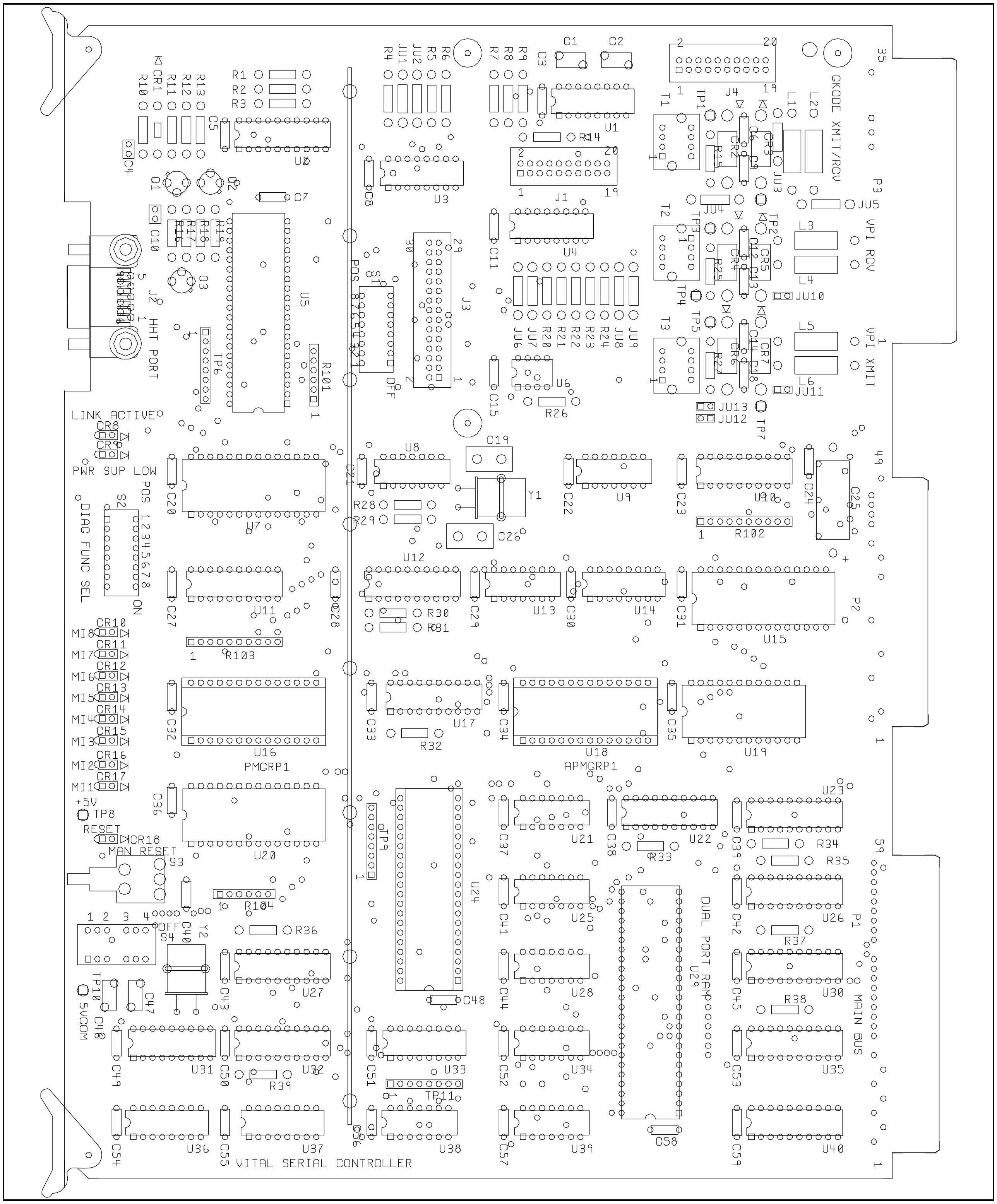

Figure B–4. VSC Board, P/N 59473-939-00

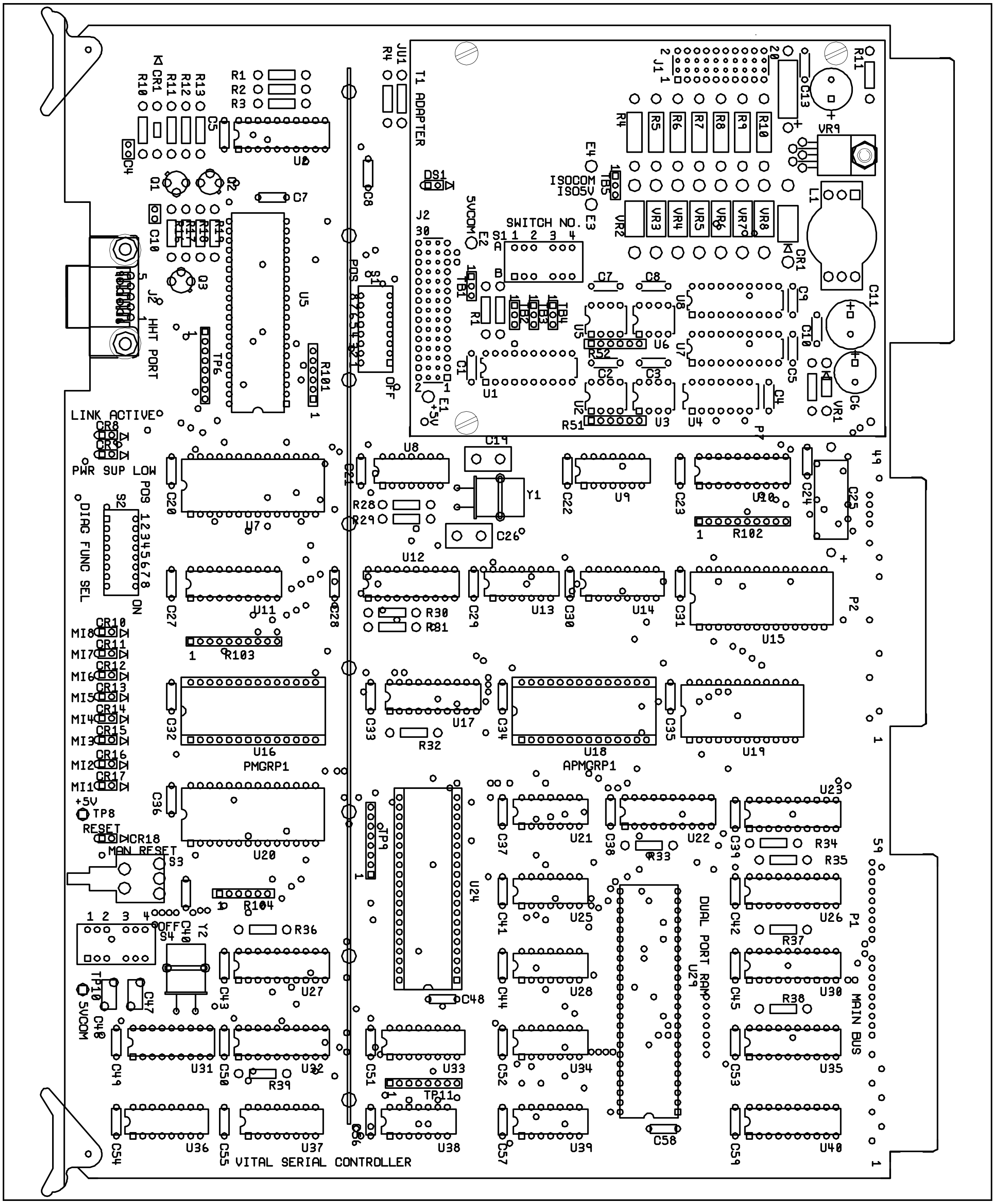

Figure B–5. VSC Board with Daughterboard, P/N 59473-939-00

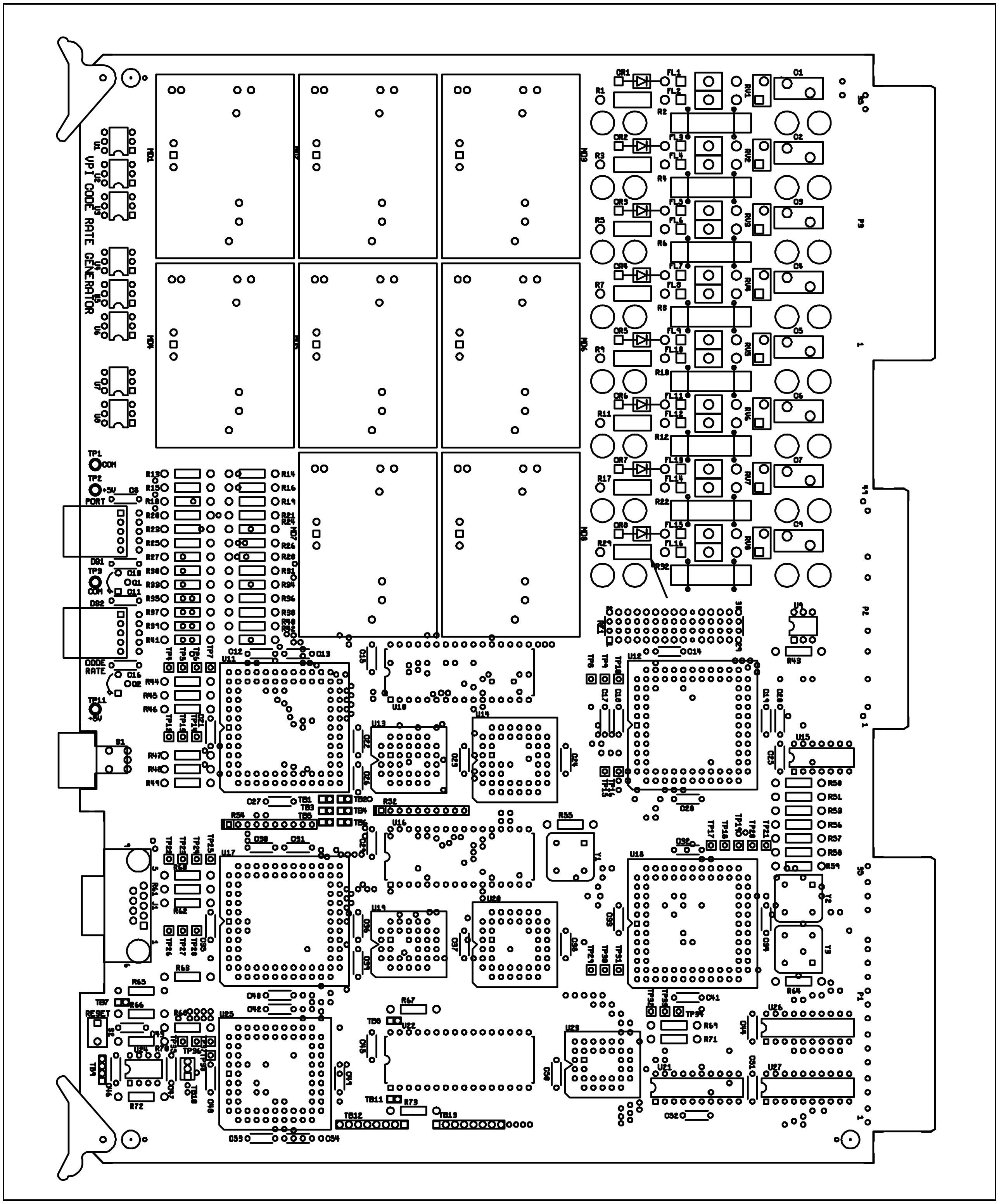

Figure B–6. CRG Board, P/N 31166-261-00

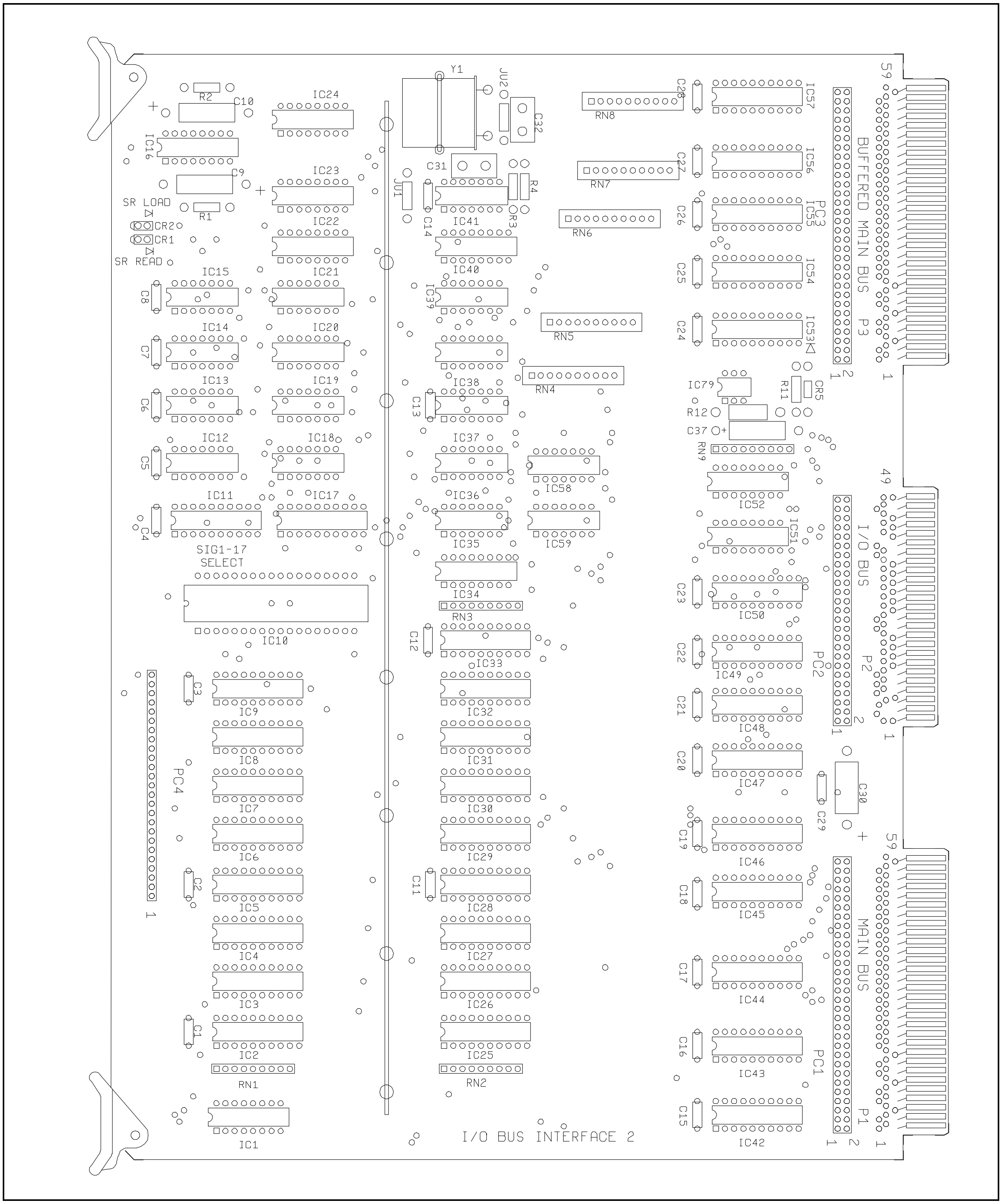

Figure B–7. IOB Board, P/N 59473-827-00

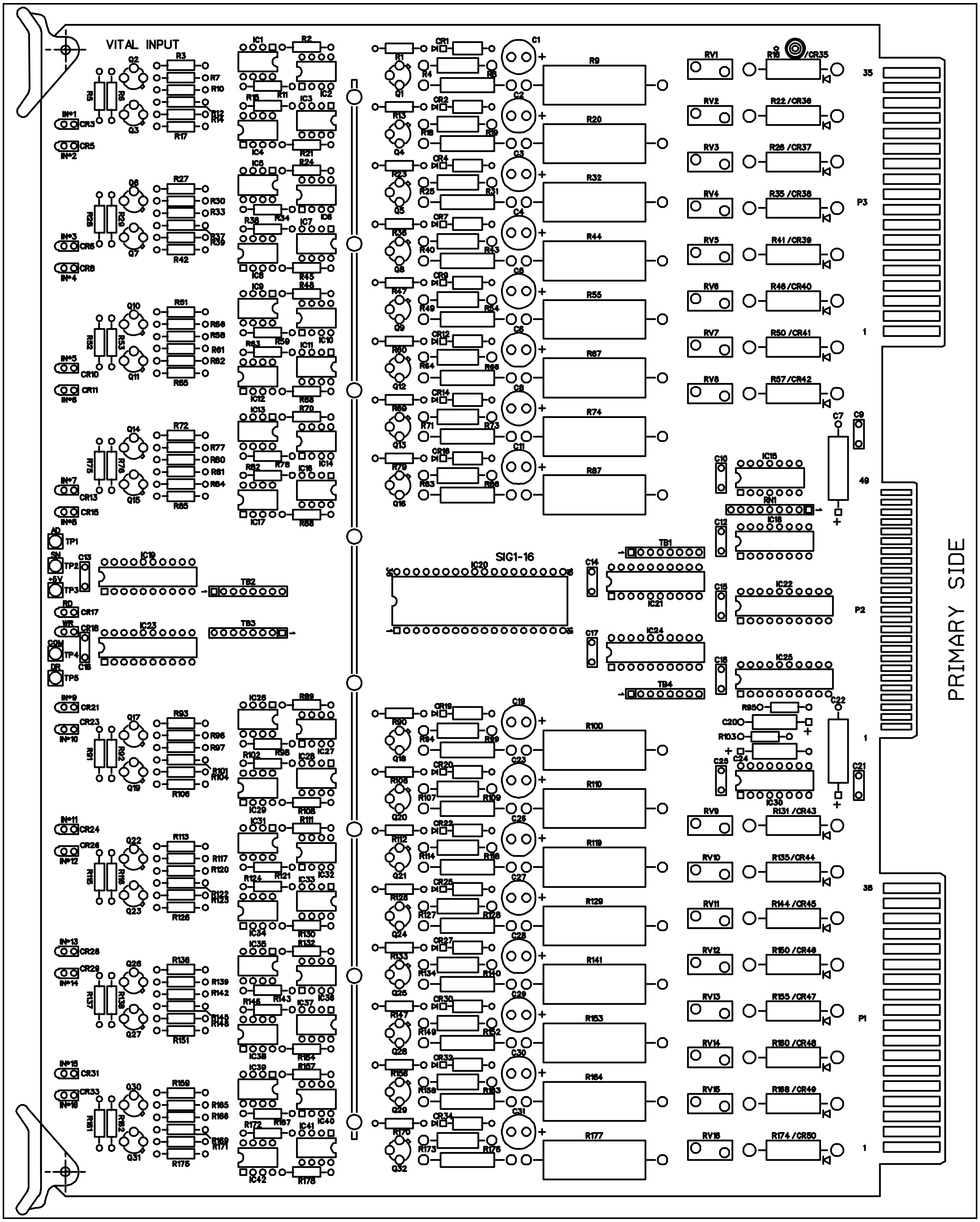

Figure B–8. DI Board, P/N 59473-867-00

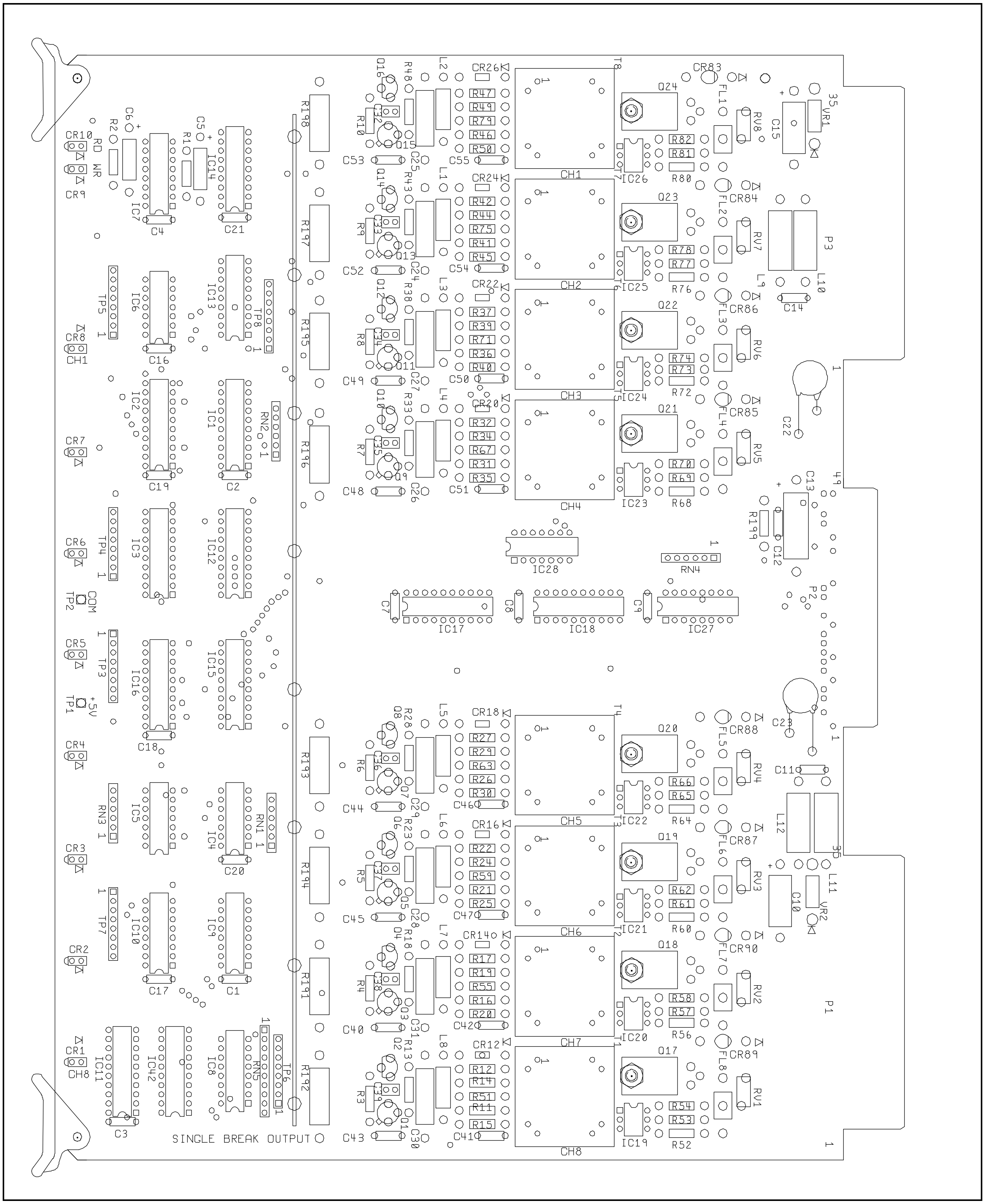

Figure B–9. SBO Board, P/N 59473-739-00

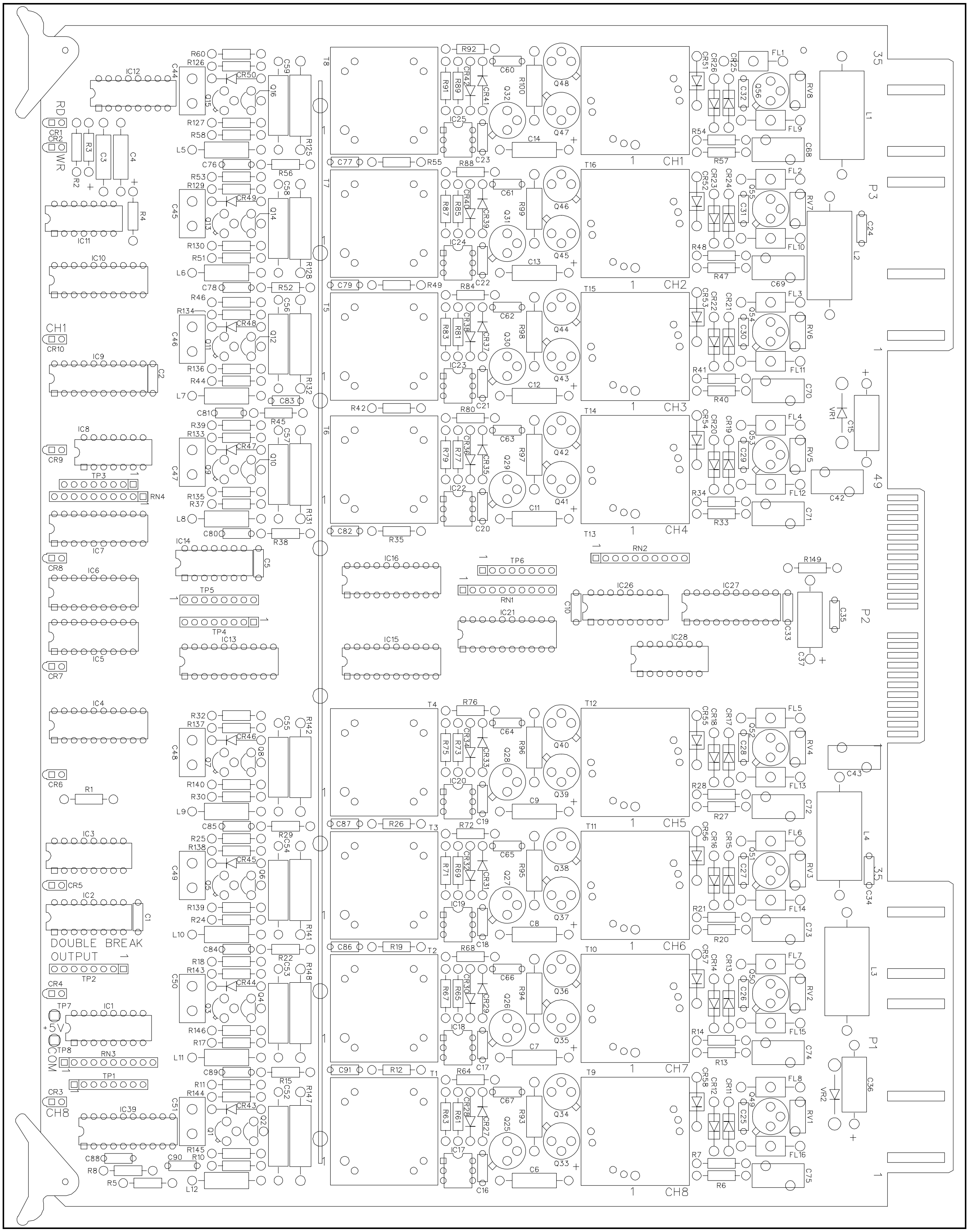

Figure B–10. DBO Board, P/N 59473-747-00

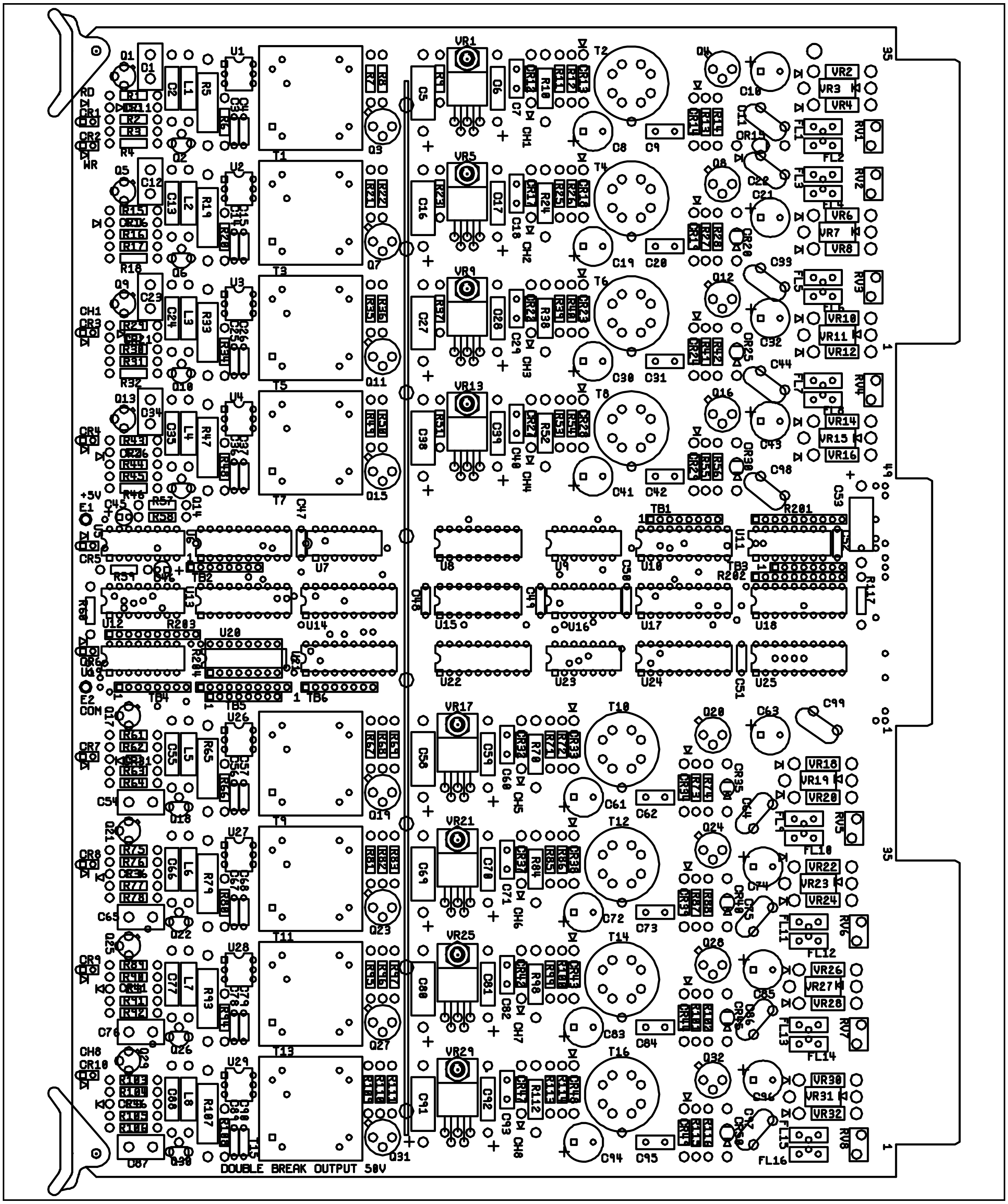

Figure B–11. DBO-50V Board, P/N 59473-977-00

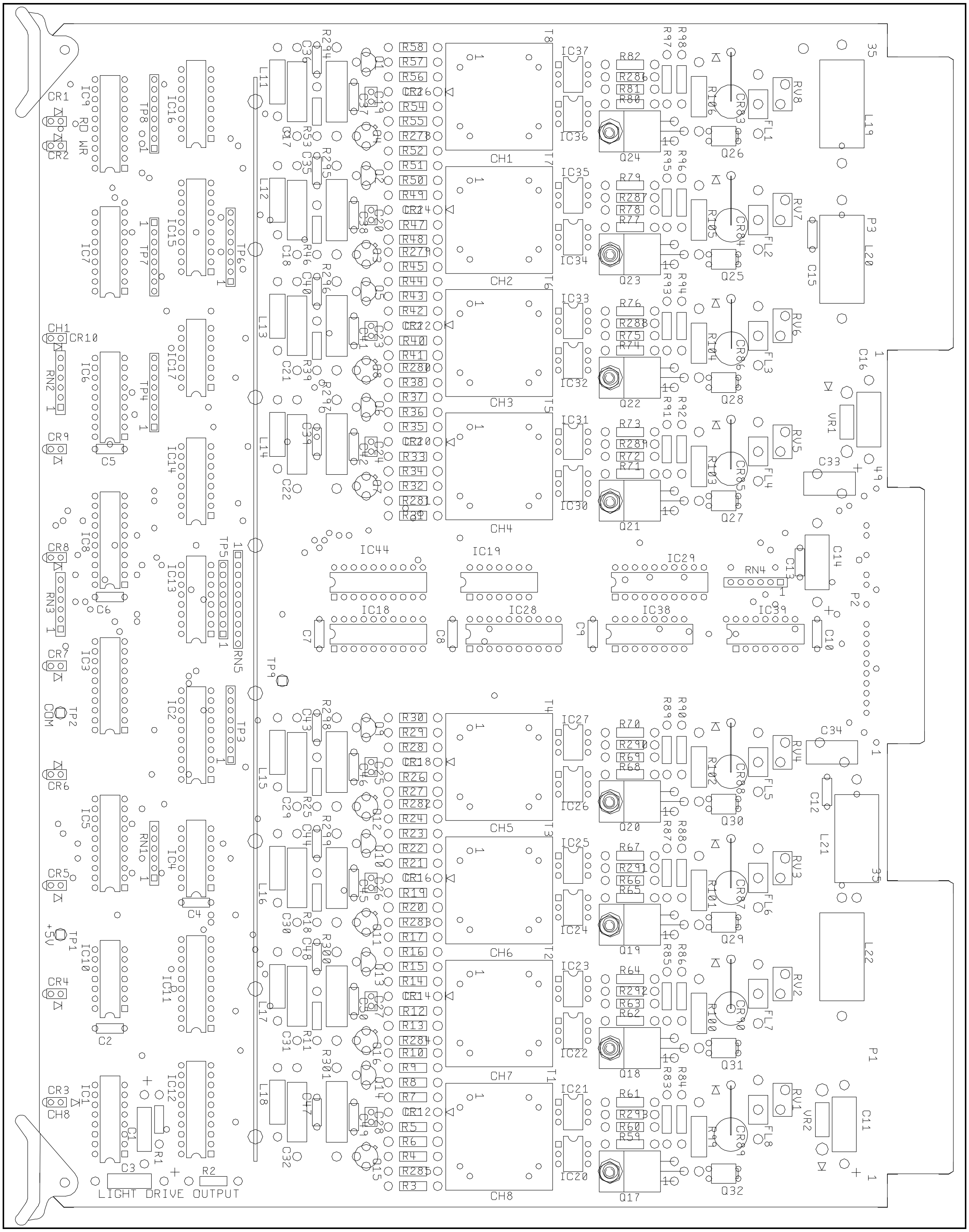

Figure B–12. LDO Board, P/N 59473-749-00

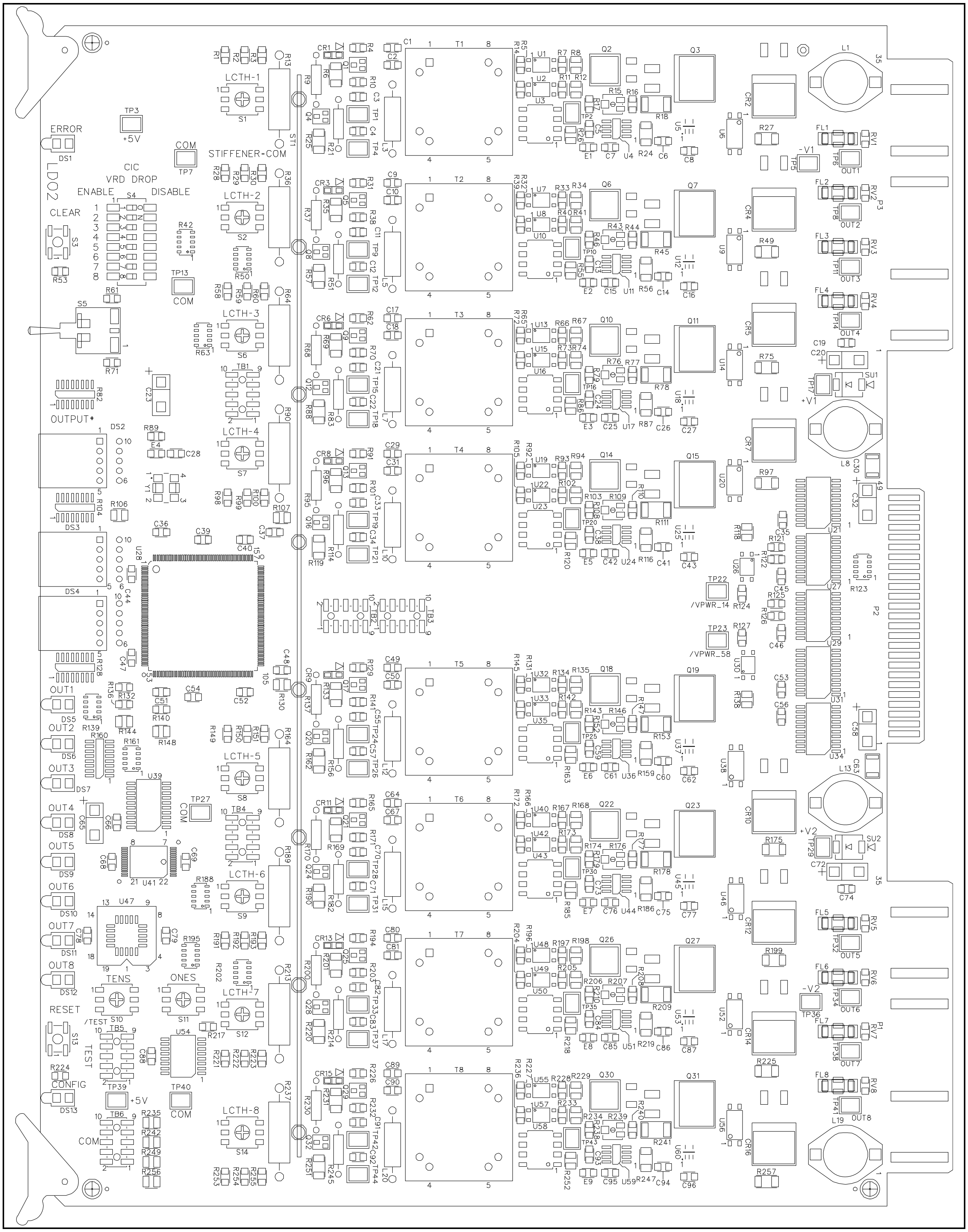

Figure B–13. LDO2 Board, P/N 31166-340-00

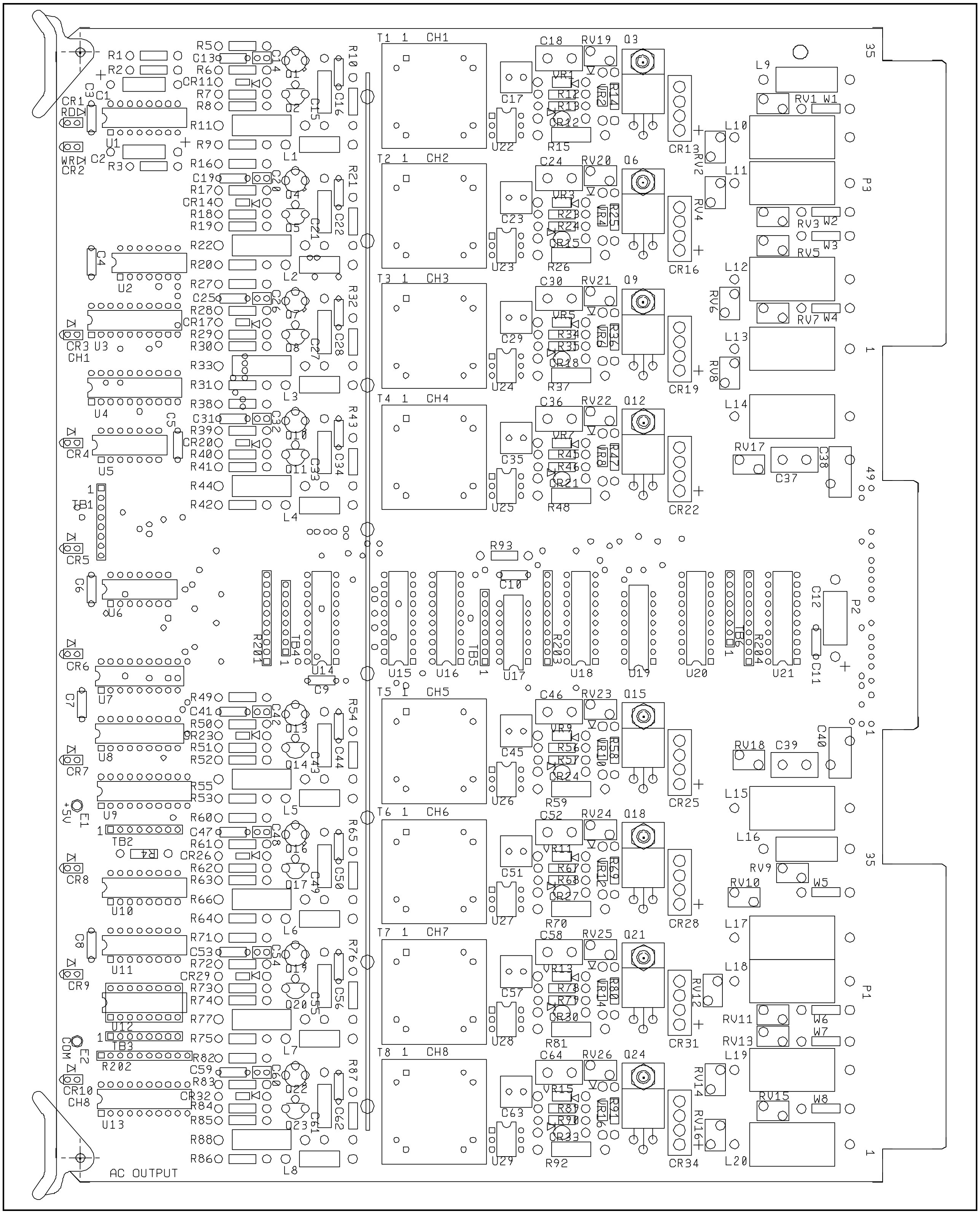

Figure B–14. ACO Board, P/N 59473-937-00

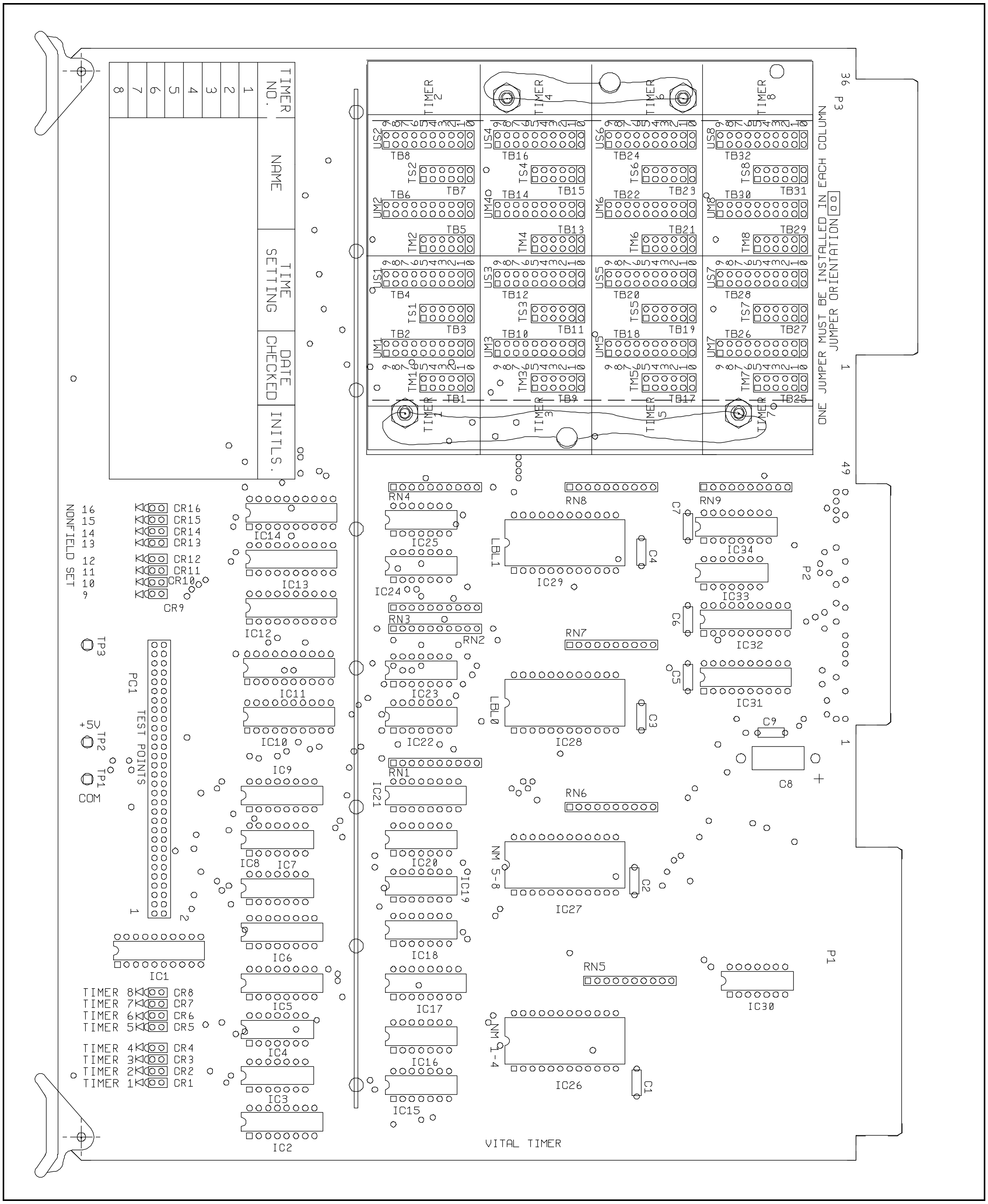

Figure B–15. FSVT Board, P/N 59473-894-00

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