



VPI[®] II

Vital Processor Interlocking Control System

Installation, Operation and Theory

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Installation, Operation and Theory Manual
P2511B, Volume 1



VPI[®] II

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PREFACE

NOTICE OF CONFIDENTIAL INFORMATION

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ABOUT THE MANUAL

This manual is intended to introduce the Alstom Vital Processor Interlocking Control System, (VPI[®] II), including an installation overview and theory of operation. This manual is part of a 5 volume set of manuals that are summarized in Section 1.

The information in this manual is arranged into sections. The title and a brief description of each section follow:

S Section 1 – GENERAL DESCRIPTION: This section describes the manual organization, introduces the topics enclosed, and introduces the VPI II system.

Section 2 – CONFIGURATION OVERVIEW, INSTALLATION AND SETUP: This section provides a general overview of the field installation and setup of the VPI II system, including capacity guidelines and allowable VSC/CSEX board combinations.

Section 3 – OPERATION: This section gives general information on the operation of the VPI II system.

Section 4 – THEORY OF OPERATION: This section provides an overview of VPI II system level functionality

Appendix A – GLOSSARY: This section provides a glossary of the terms used in the 5 volumes of this manual set.

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MANUAL SPECIAL NOTATIONS

In the Alstom manuals, there are three methods used to convey special informational notations to the reader. These notations are warnings, cautions, and notes. Both warnings and cautions are readily noticeable by boldface type two lines beneath the caption.

Warning

A warning is the most important notation to heed. A warning is used to tell the reader that special attention needs to be paid to the message because if the instructions or advice is not followed when working on the equipment then the result could be either serious harm or death. The sudden, unexpected operation of a switch machine, for example, or the technician contacting the third rail could lead to personal injury or death. An example of a typical warning notice follows:

WARNING

DISCONNECT MOTOR ENERGY WHENEVER WORKING ON SWITCH LAYOUT OR SWITCH MACHINE. UNEXPECTED OPERATION OF MACHINE COULD CAUSE INJURY FROM OPEN GEARS, ELECTRICAL SHOCK, OR MOVING SWITCH POINTS.

Caution

A caution statement is used when an operating or maintenance procedure, practice, condition, or statement, which if not strictly adhered to, could result in damage to or destruction of equipment. A typical caution found in a manual is as follows:

CAUTION

Turn power off before attempting to remove or insert circuit boards into a module. Boards can be damaged if power is not turned off.

Note

A note is normally used to provide minor additional information to the reader to explain the reason for a given step in a test procedure or to just provide a background detail. An example of the use of a note follows:

NOTE

A capacitor may be mounted on the circuit board with a RTV adhesive. Use the same color RTV.

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1. SECTION 1 – GENERAL DESCRIPTION

1.1. INTRODUCTION

This document contains a general description of the Alstom VPI[®] II Vital Processor Interlocking Control System. It contains basic system level information, technical hardware descriptions, maintenance and troubleshooting instructions.

The technical material in this manual assumes the reader has a basic knowledge of railroad signaling terminology, digital electronics and basic computer software principles. Courses are available for the user that requires additional training. Contact an Alstom representative for details.

1.2. GENERAL

This section describes the manual organization, introduces the topics enclosed, and introduces the VPI II system.

1.3. TERMS, ABBREVIATIONS AND TRADE NAMES

Terms and abbreviations used throughout this manual are defined in Appendix A. Refer to Appendix A anytime a term or abbreviation in the text is unfamiliar.

GenTraCode[®] and VPI[®] are registered trade names of Alstom Signaling Inc, while cTc[™] and Safety Assurance Logic[™] are trademarks of Alstom Signaling Inc.

1.4. MANUAL SET ORGANIZATION

This manual is part of a 5 volume set supporting the VPI II system. The set is organized as follows:

- Volume 1, Installation, Operation, and Theory Manual, is this document. It includes general overview of the field installation and setup of the VPI II system; including capacity guidelines and allowable VSC/CSEX board combinations, system operation, and theory of operation.
- Volume 2, Chassis Configuration, describes the chassis configuration including cables and power supplies.
- Volume 3, Vital Subsystem, includes the Vital subsystem board drawings, signature headers and proms, and board reference data.
- Volume 4, Non-Vital Subsystem, includes non-vital subsystem board drawings and board reference data.

- Volume 5, Maintenance and Troubleshooting, describes system maintenance and troubleshooting, including discussion of diagnostics and references for the applicable software and hardware manuals.

1.5. RELATED PUBLICATIONS

Several additional publications pertain to the VPI II system:

- P2511A, VPI II Product Overview
- P2346, Series: Code/Communication System Publications
- P2509, Maintenance Management System (MMS)
- P2412A, CAAPE Users Guide
- P2412B, CAAPE AlsDload
- P2412D, VPI CAA Reference
- P2412E, DataLogger

1.6. VPI II SUBSYSTEMS

The VPI II system is comprised of five main parts as shown in Figure 1–1.

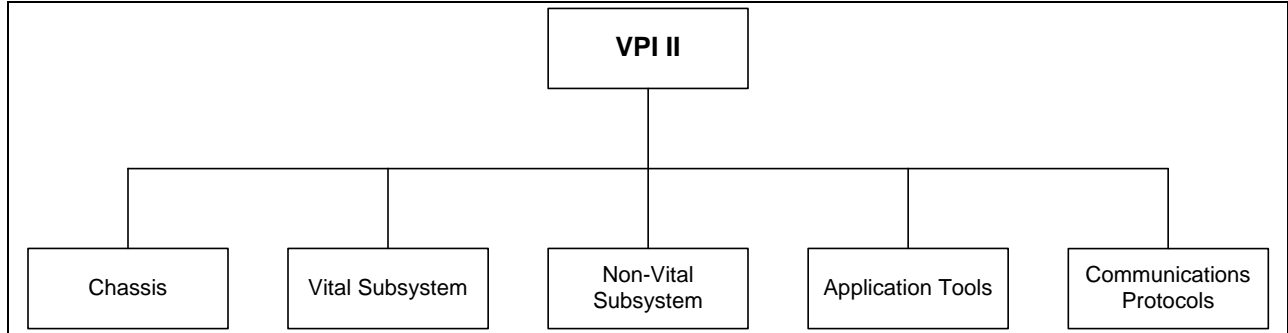


Figure 1–2. VPI II Breakdown

This hardware manual focuses primarily on the Chassis, Vital Subsystem and Non-Vital Subsystem.

1.7. VPI II SYSTEM FEATURES

The VPI II module is a Vital fail-safe, microprocessor-based control system designed to meet the needs of interlocking control for mainline railroads and mass transit applications.

Designed as a modular control system, it contains a set of plug-in Printed Circuit Boards applied in varying quantities to meet the needs of a specific project. Although one VPI II system is sufficient for many installations, additional systems in distributed arrangements are available for sites that have specific availability or configuration requirements. A single VPI II system may include 1 to 4 chassis depending on I/O arrangements. Single VPI II systems controlling interlockings with 35 point machines have been proposed. The VPI II system is based on VPI system, the largest single VPI system installed so far has 20 points machines and the average number of point machines per system tends to be less due to specific project availability requirements.

The VPI II system is fully compatible with the majority of equipment found at interlockings. Figure 1–2 shows how a control center, through the DC code line/communications system, interfaces with more than one Vital interlocking and shows the ancillary features that can be added to the basic VPI II system. In addition, other viable ways of communication from the Central Control are via microwave, radio and fiber optic links. Figure 1–3 shows some examples of equipment commonly operated under VPI II control.

NOTE

A VPI II System performing non-vital functions can be configured with either a Code System Emulator Extended 3 or 4 (CSEX3 or CSEX4) non-vital processor board. This manual uses the generic term CSEX unless a function is specific to CSEX3 or CSEX4. See P2511B, Volume 4 for discussions of the two boards.

The VPI II system can be mounted in a small, wayside equipment shelter. No special heating or cooling equipment is required for operation in AREMA-specified environments of Class C or Class D (-40 to +70 degrees C). Built-in secondary transient protection is provided for all I/O lines to prevent disruption of service from electromagnetic interference (EMI) such as lightning or other local interference. If required, additional primary protection devices can be added to the external lines to protect against higher level EMI such as pulses from nearby electrical storms. Typically, no interface devices are required between the VPI II inputs and outputs and the standard interlocking appliances

Inputs to the VPI II system are identical to older, Vital relay-based systems. No relays are used in the solid-state module, thereby eliminating the need for periodic maintenance or adjustments. With VPI II, complex relay logic is:

- reduced to a closed set of Boolean mathematical expressions, or
- expressed as Relay Logic Diagrams representing standard relay contact closures

Then, through Alstom's Computer-Aided Application Programming Environment (CAAPE) software package, these Boolean expressions are converted into operating instructions for the VPI II microprocessor. Both Vital and non-vital applications are created with the same user interface. The CAAPE software package is also used to configure the hardware of the VPI II chassis.

The tool set includes a graphical simulator that allows the signal engineer to exercise the logic before building the hardware. The simulator provides a mechanism for the signal engineer to demonstrate the operation of the interlocking before the design is complete. As such, it can offer clarifying detail to design reviews. The simulator can also be used in presenting the application design to non-signaling personnel, e.g., operating personnel, to insure that the signal design adequately supports the operational needs.

The VPI II system has separate subsystems for Vital and non-vital control. The Vital and non-vital logic and hardware are maintained as separate subsystems to allow modifications in one section to not affect the other. These subsystems can share a chassis or be configured in separate chassis. Refer to Figure 1–2 for a general block diagram of a portion of a control system with two VPI II systems.

General Description

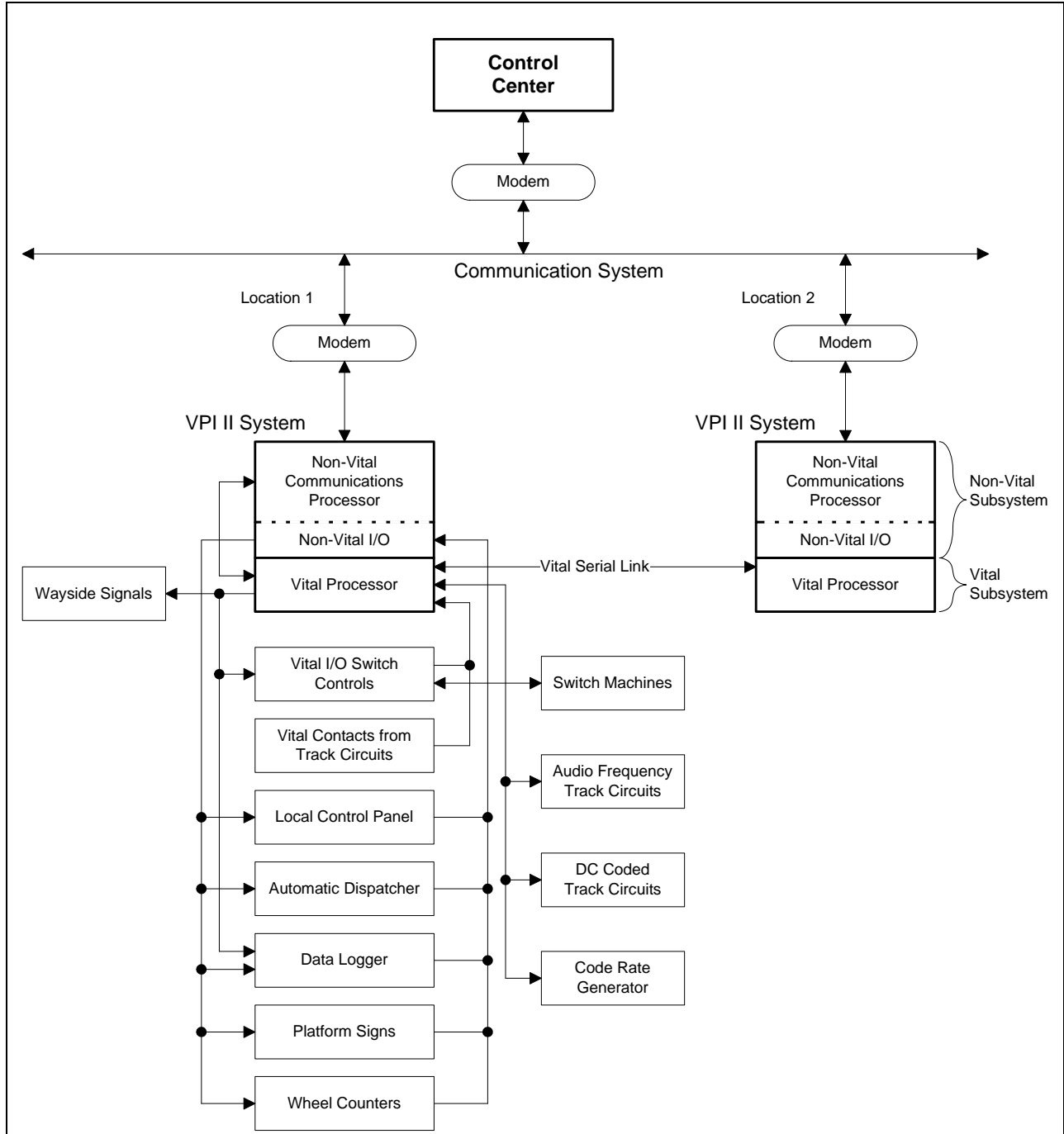


Figure 1-2. General VPI II System Block Diagram

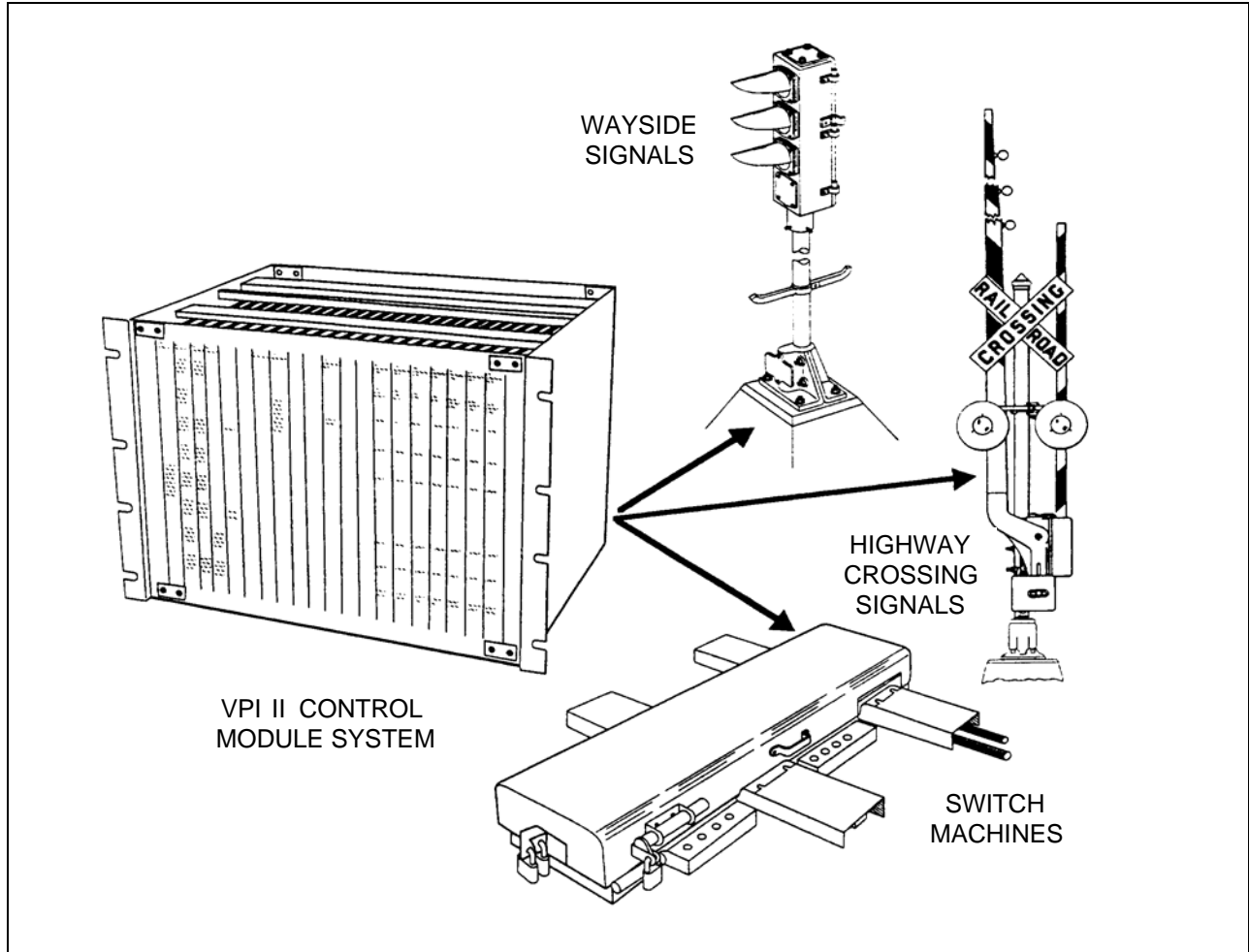


Figure 1-3. Typical Wayside Devices Under VPI II Control

1.8. SPECIFICATIONS

Table 1–1 lists nominal specifications for the VPI II module.

Table 1–1. VPI II Specifications

Characteristic	Specification
Logic Input Power	5 ± 0.25 VDC at 8 amperes maximum per module
High Voltage Isolation Rating	Meets AREMA Wayside Class C and Class D requirements
Operating Temperature	-40 to +160°F (-40 to +70°C) Meets AREMA Wayside Class C and Class D requirements
Humidity	0 to 95% Non-Condensing Meets AREMA Wayside Class C and Class D requirements
Vibration	5-20 Hz: 0.07" p-p 20-200 Hz: 1.5g p Meets AREMA Wayside Class C and Class D requirements
Shock	Shipping: 10 g p Operating: 10 g p Meets AREMA Wayside Class C and Class D requirements
Typical Weight per Module with some boards	15 lbs. (6.80 kg)
Dimensions	14H × 19W × 23D* inches (35.6H × 48.3W × 58.5D cm)

* Depth includes cable dress at rear of chassis

1.9. DIAGNOSTICS

Four diagnostic support alternatives exist for troubleshooting a VPI II system. They are for remote and local testing:

- LEDs on circuit boards for visual operating checks
- AlsDload Software Download program used to download application data structures and system software
- Maintenance Management System (MMS), a graphical Diagnostic and Maintenance Application that uses a graphical Track Layout to dynamically record and display the VPI II diagnostic status, the status of linked VPI II variables and play recorded data.

In addition, a properly equipped data terminal is used for non-vital system diagnostics.

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2. SECTION 2 – CONFIGURATION OVERVIEW, INSTALLATION, AND SETUP

2.1. INTRODUCTION

This section provides a general overview of the field installation and setup of the VPI II system, including capacity guidelines and allowable VSC/CSEX board combinations.

2.2. GENERAL

The installation process includes configuration of the software of the VPI II system for regular service. Initial checkout procedures are given at the end of the section to verify proper system performance.

The maintainer should be aware of the specific rules about board placement and board combination within a VPI II system. These rules are summarized in Table 2–1 through 2-4. These rules are considered when Alstom configures a VPI II system for an application.

The VPI II system is supplied as part of a packaged, pre-assembled, control system that is mounted in a rack frame. The installation instructions for a stand-alone device, in the event the VPI II module is added to an existing system or is used to replace a damaged unit, are included in this section.

WARNING

DISRUPTION OF VITAL CONTROLLER SERVICE POSES A POTENTIAL THREAT TO RAIL SAFETY. BEFORE SHUTTING DOWN A FACILITY FOR ANY REASON, NOTIFY THE RAILROAD DISPATCHER IN CHARGE OF THE AFFECTED ROUTE(S). TAKE ALL STEPS NECESSARY TO ENSURE THE SAFE PASSAGE OF TRAFFIC IS MAINTAINED.

2.3. CAPACITY OVERVIEW

This topic explains the VPI II capacity guidelines.

Several factors dictate how large an application one VPI II system can handle. Due to the various hardware configurations and application logic requirements, it can be difficult to determine before design completion whether the application size exceeds that which one system can properly execute. However, there are criteria available that define when an upper boundary is approached. A general guideline for estimating the capacity of an applied VPI II system is based on the system processor board, the CPU II board. Processing time estimates can be made using a spreadsheet with the VPI II CAA. Consult Alstom if a more exact system estimate is required than the general guidelines provide.

2.3.1. Hardware Criteria

For the largest applied system there are certain limits concerning the number of certain printed circuit boards that may be used. Board usage limits are fixed by the module form factor while others are established by system processing. Table 2–1 through 2-3 list boards by board type and the maximum number of boards allowed per VPI II system.

Table 2–1. Vital Board Hardware Criteria

Vital Board Type	Boards Per System
CPU II	1 board/system
VRD	1 board/system
I/O Bus Interface 14 Vital addresses per/Vital I/O group	1 board/Vital I/O group
Vital Inputs (all types) 16 Inputs/board 1 Vital Address/board	20 boards/system
Vital Timer 8 Field-settable Timers/board 1 Vital Address/board	2 boards/system
Vital Outputs (all types) 8 Outputs/board 1 Vital Address/2 boards	40 boards/system
Vital Serial Communications (VSC)	10 - (#VSC + #MVSC + #GVSC + #GVSCE + #CRG + #CSEX)
Multidrop Vital Serial Communications (MVSC)	2 - (#GVSC + #GVSCE)
Genrakode Vital Serial Communications (GVSC)	2 - (#MVSC + #GVSCE)
Genrakode Vital Serial Communications Extended (GVSCE)	2 - (#GVSC + #MVSC)
Code Rate Generator (CRG)	3

Table 2–2. Non-Vital Board Hardware Criteria

Non-Vital Board Type	Boards Per System
CSEX (3 or 4)	4 boards/system
Non-Vital I/O (including TWC boards)	20 boards/CSEX subsystem
NVTWC Modem NVTWC Multiplexer NVTWC FSK	8 boards of these combinations/CSEX subsystem

Table 2–3. Board Limits / Application Criteria

Board Limits	CPU II
Vital Equation size per system (Quantity dependent upon average expression complexity)	2000 to 3000 Boolean equations
Maximum product terms/Vital equations	63
Maximum parameters/product terms	63
Vital Software Timers	300 per system
CPU-to-VSC Parameters	200 per VSC subsystem
VSC-to-CPU Parameters	200 per VSC subsystem
CPU -to-GVSC Parameters	450 per GVSC subsystem
GVSC-to-CPU Parameters	450 per GVSC subsystem
CPU -to-GVSCE Parameters	450 per GVSC subsystem
GVSCE-to-CPU Parameters	450 per GVSC subsystem
CPU -to-MVSC Parameters	450 per MVSC subsystem
MVSC-to-CPU Parameters	450 per MVSC subsystem
CPU -to-CRG Parameters	80 per CRG subsystem
CRG-to-CPU Parameters	8 per CRG subsystem
CPU-to-CSEX Parameters	800 per CSEX subsystem
CSEX-to-CPU Parameters	400 per CSEX subsystem
Non-Vital Equation size	4000 per CSEX subsystem
Non-Vital Software Timers	200 per CSEX subsystem

Note 1: CPU II boards cannot simultaneously use all features at maximum limits. Therefore, when planning for system capacity, it is mandatory to consider processing time plus application Flash and system RAM limits.

Note 2: There is a system-wide limit of 759 CSEX-to-CPU parameters independent of distribution on CSEX boards.

2.4. VSC/CSEX BOARD COMBINATIONS

There are specific acceptable VSC /CSEX board combinations and board placement rules applicable for the VPI II system. The acceptable combinations are summarized in Table 2–4.

If more than four VSC-type boards are located in a single module, their board addresses are taken from the CSEX address range and the maximum number of CSEX boards in that module is reduced. For example, if six VSC-type boards are located in a particular module, only two CSEX boards are placed in that module.

Table 2–4. Allowable VSC/CSEX Board Combinations

Total Number of VSC Type Boards	Allowable CSEX Boards: System Module	Allowable CSEX Boards: Expansion Module	Allowable VSC Type Boards: System Module	Allowable VSC Type Boards: Expansion Module
0	4	4	-	-
1	4	4	1	0
	4	4	0	1
2	4	4	2	0
	4	4	1	1
	4	4	0	2
3	4	4	3	0
	4	4	2	1
	4	4	1	2
	4	4	0	3
4	4	4	4	0
	4	4	3	1
	4	4	2	2
	4	4	1	3
	4	4	0	4

Table 2–4. Allowable VSC/CSEX Board Combinations (Cont.)

Total Number of VSC Type Boards	Allowable CSEX Boards: System Module	Allowable CSEX Boards: Expansion Module	Allowable VSC Type Boards: System Module	Allowable VSC Type Boards: Expansion Module
5	3	4	5	0
	4	4	4	1
	4	4	3	2
	4	4	2	3
	4	4	1	4
	4	3	0	5
6	2	4	6	0
	3	4	5	1
	4	4	4	2
	4	4	3	3
	4	4	2	4
	4	3	1	5
	4	2	0	6
7	1	4	7	0
	2	4	6	1
	3	4	5	2
	4	4	4	3
	4	4	3	4
	4	3	2	5
	4	2	1	6
	4	1	0	7

Table 2–4. Allowable VSC/CSEX Board Combinations (Cont.)

Total Number of VSC Type Boards	Allowable CSEX Boards: System Module	Allowable CSEX Boards: Expansion Module	Allowable VSC Type Boards: System Module	Allowable VSC Type Boards: Expansion Module
8	0	4	8	0
	1	4	7	1
	2	4	6	2
	3	4	5	3
	4	4	4	4
	4	3	3	5
	4	2	2	6
	4	1	1	7
9	0	4	8	1
	1	4	7	2
	2	4	6	3
	3	4	5	4
	4	3	4	5
	4	2	3	6
	4	1	2	7
	4	0	1	8
10	0	4	8	2
	1	4	7	3
	2	4	6	4
	3	3	5	5
	4	2	4	6
	4	1	3	7
	4	0	2	8

2.5. UNPACKING AND INSPECTION

Carefully open the shipping carton and check the contents against the packing list secured to the outside of the container. Accessories and spare parts kits are wrapped separately. Take careful note of all small hardware shipped with the units. Inspect all items for signs of damage. Save all packing material for possible re-shipment.

2.6. MOUNTING PROCEDURES

Each VPI II installation differs slightly depending on the type of rack enclosure used and the types of equipment to be controlled. While it is impossible to anticipate all mounting configurations, the procedure in Table 2–5 is intended as a guide for typical systems. Refer to the rack mount illustration shown in Figure 2–1 for these procedures.

Table 2–5. VPI II Mounting Procedure

Step	Procedure
1	Install, if required, clip-on nuts at the rack holes for VPI II module mounting.
2	Line up the holes on the front panel of the VPI II module with the mounting holes/nuts in the rack frame. Secure the module to the rack with screws as shown.
3	Connect the VPI II ground wire.
4	Connect all rear panel cables (if applicable) as required by the system plans (see Figure 2–2 for an example). Tighten the retaining screws or clips (if so equipped) on the cable plugs to secure them to the VPI II rear panel. Dress all cabling in accordance with the system plans. <u>NOTE</u> Some VPI II racks may have either 18 or 32 volt AC heavy-duty surge protectors mounted on a panel to handle unwanted line surges.

2.7. PRE POWER-UP CHECKS

Once the equipment is mounted, and before application of power, perform the procedure provided in Table 2–6.

Table 2–6. VPI II Pre Power-up Checks Procedure

Step	Procedure
1	Verify that any power supplies, batteries and chargers used with the VPI II system adhere to operating specifications. The VPI II logic power supply, if other than provided by Alstom, should be 5 VDC ($\pm 0.25V$, 1% ripple) and must meet AREMA isolation requirements, as found in AREMA Specification Section 11.5.1 if the primary energy source is Vital.
2	Verify VRD relay and repeaters are securely fastened to the relay plugboards. The system cannot operate if this is not done.
3	Check all output wiring for shorts to avoid possible damage to the system outputs. Check all power connections for the correct voltage and polarity.
4	Lower the VPI II front cover plate and verify that all plug-in printed circuit boards are firmly seated in the correct slots.
5	Verify that Signature PROMs & Signature Headers are in place and in proper order per module arrangement plan.

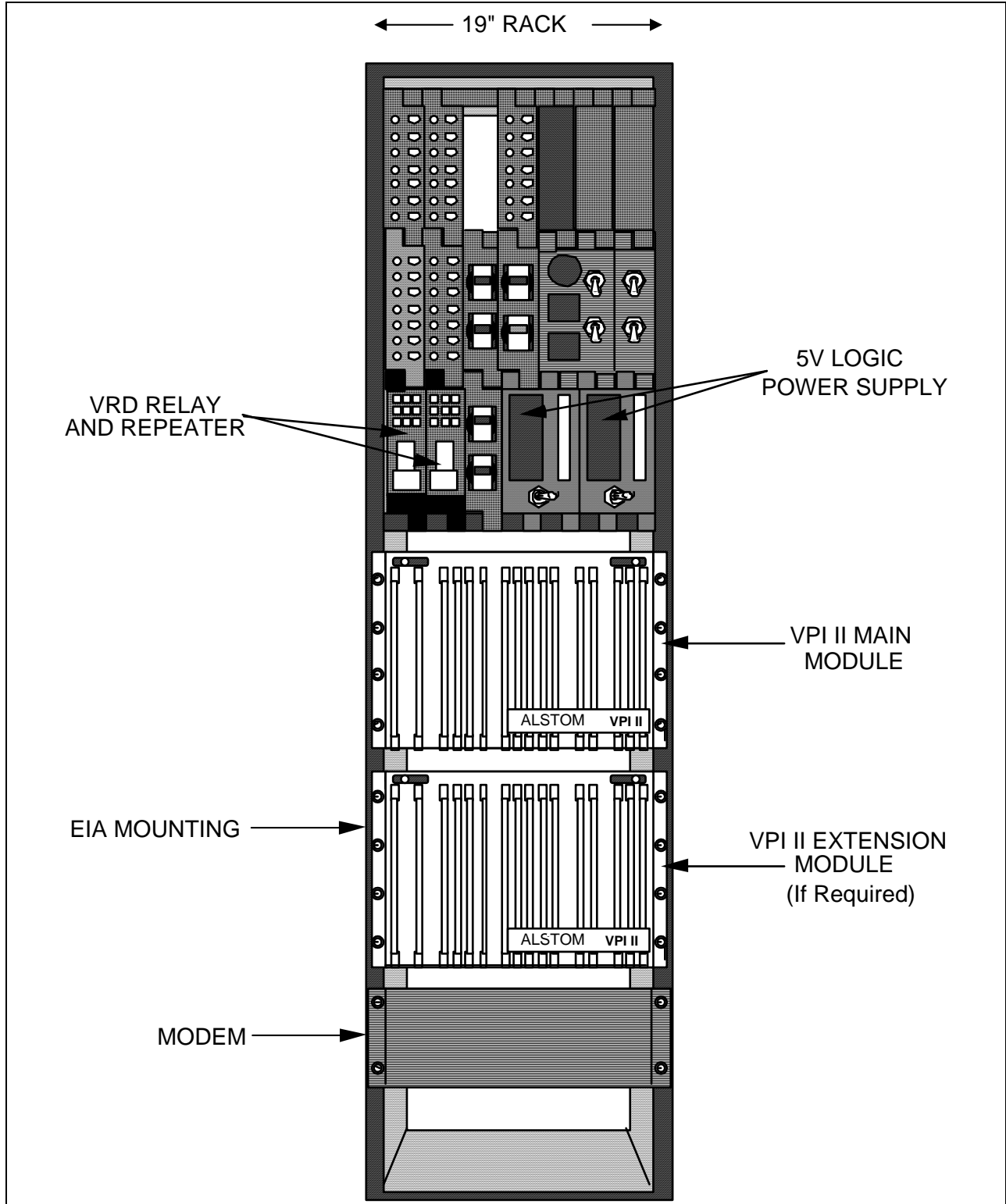


Figure 2-1. Typical Rack Mount Installation

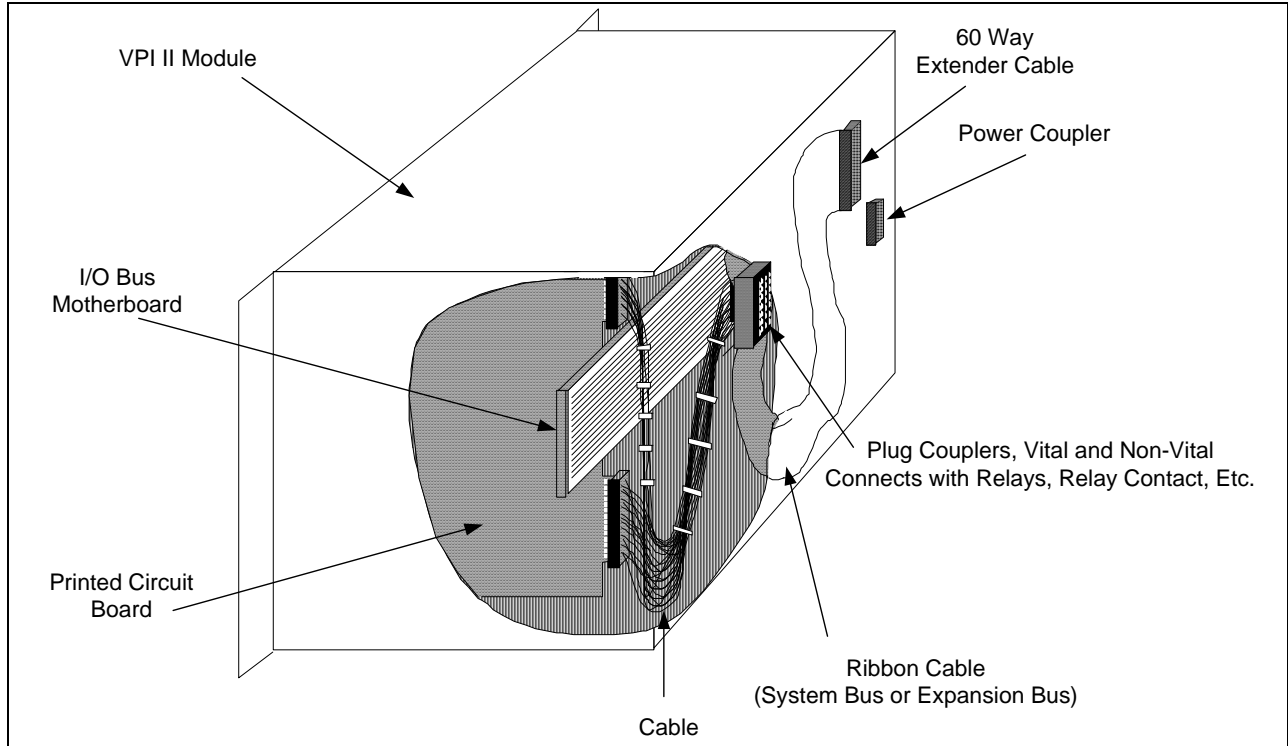


Figure 2-2. Typical Module Rear Panel Wiring with Plug Coupled Chassis

2.8. SOFTWARE CONFIGURATION

Before activating a VPI II module, configure the interlocking logic to meet the needs of the particular installation. To configure the logic, use a PC with Alstom's Computer-Aided Application Programming Environment (CAAPE) software. The CAAPE software is used to program the VPI II's Flash (programmable read only memory used with embedded processors, see Appendix A). For instructions on using the CAAPE package, refer to the CAAPE's on-line help. See P2512B for detail about using the AlsDload Software Download Program to program a CPU II board without removing the board from the system.

While the VPI II Vital system software is common to all installations, the application data structure, which describes the logical operation of a specific interlocking, needs to be customized for each location. These Boolean equations or Relay Logic Diagrams are written by the Application or Signal Engineer using the CAAPE software in conjunction with traditional tools such as a track plan and aspect charts. These equations may also be written as a direct interpretation of existing relay logic circuits. After the equations are written, the logic can then be tested and loaded into Flash.

2.8.1. AlsDload Software

The Alstom AlsDload software utility, a part of CAAPE, is used to program application data structures and system software. It can be used to download software or configure a system. For detailed information about AlsDload, refer to Alstom publication P2512B.

2.9. RECORDING OF SYSTEM CONFIGURATION DATA

Whenever a new or modified VPI II system is put into service, the system configuration data should be recorded using the ".CFG" report generated by the CAAPE. This provides a means to verify that the CAAPE instructions exactly match the Flash contents residing on the Vital system boards.

Although not strictly required, it is recommended that during other (non-VPI or non-VPI II) periodic maintenance programs the VPI II configuration data be re-recorded and verified against the installed/in service configuration data. This ensures that the on-site documentation reflects current configuration and is kept up to date. This data can be accessed by using Alstom MMS software. AlsDload can be used to download an application to a CPU II board and obtain signatures and addresses from a CPU II board. MMS and AlsDload are discussed further later in this document.

Use the form provided in Figure 2–3 to log the configuration data. The form may be locally reproduced as needed.

SOFTWARE CONFIGURATION DATA LOG		
Name of Person Performing System Query: _____		
Location of System: _____		
System Description (e.g. SYSTEM 1 or MAIN SYSTEM or application name): _____		
IN SERVICE		
Date: _____		
Current Date: _____		
Following "R" Command: _____		
INPUT FILE #: _____		
CAAPE FILE #: _____		
VRS FILE #: _____		
	INPUT FILE NUMBER	RUNTIME/DATE
VSC.VB1		
VSC.VB2		
VSC.VB3		
VSC.VB4		
VSC.VB5		
VSC.VB6		
VSC.VB7		
VSC.VB8		
VSC.VB9		
VSC.VBA		
	VRS FILE NUMBER	REVISION
CRG 1		
CRG 2		
CRG 3		
Following "Q" Command:		
System Software Signature @ ADDR 124 _____		
Application Signature @ ADDR 128 _____		

Figure 2–3. Logic Configuration Log Sheet for CPU II Board Assembly

2.10. GENERAL DIAGNOSTICS

Using a PC with AlsDload software or MMS connected to the CPU II board, apply VPI II system power and observe the display screen:

- If operation is correct, “SYSTEM OK” is displayed and the VRD relay energizes after several seconds.
- If connections to system inputs or outputs are open or intermittent, the “SYS WARNING” message may be observed. This type of failure may still allow the VRD relay to energize.
- If a major fault is detected, the display reads “ERROR ALERT.” The VRD relay remains de-energized in such cases.
- If the VRD relay remains de-energized and no display message is shown, verify that the application memory has been properly configured and installed on the CPU II and that the PC is properly connected. If the failure persists, refer to P2511B, Volume 5, Maintenance and Troubleshooting, for in-depth troubleshooting procedures.
- If an “ERROR ALERT” or “SYS WARNING” display is shown, refer to P2511B, Volume 5, Maintenance and Troubleshooting, for in-depth troubleshooting procedures.

2.11. ALSDLOAD SOFTWARE

The Alstom AlsDload software utility is used to configure the system software and application on a CPU II board. It also is used to verify a configuration as compared to a specific application. For detailed information about AlsDload, refer to Alstom publication P2512B.

2.12. VITAL DIAGNOSTIC PROTOCOL (VDP)

Using Alstom’s optional Vital Diagnostic Protocol (VDP), a user may view CPU II board status and perform CPU II diagnostic commands when connected to the non-vital CSEX board’s Maintenance Access (MAC) port. For detail on the VDP, refer to Alstom publication P2346W and P2511B, Volume 5, Maintenance and Troubleshooting.

2.13. MAINTENANCE MANAGEMENT SYSTEM (MMS)

The Maintenance Management System (MMS) is a diagnostic tool used to remotely monitor both the Vital and non-vital subsystems of each VPI II location. MMS runs on a PC under a variety of operational systems. Contact Alstom for a complete list of supported operating systems.

For detailed information regarding MMS operation, refer to Alstom publication P2509 and Section 5 of P2511B, Volume 5.

3. SECTION 3 – OPERATION

3.1. INTRODUCTION

This section gives general information on the operation of the VPI II system.

3.2. START-UP PROCEDURE

The VPI II system requires no warm-up period; it may be used immediately after being turned on. Simply apply system power to the module to begin Vital controller operation. The power switch is typically located on or near the rack structure.

3.3. OPERATING INSTRUCTIONS

The VPI II system is designed for automatic, unattended field operation. Once power is applied, operator actions are limited to infrequent, periodic observation to ensure that proper interlocking operation is maintained. Included with many installations is an indication and control panel (or local control panel) that can be used to observe and activate basic interlocking functions. In addition, the Alstom MMS can be used to remotely, continuously monitor one or several VPI II installations (refer to Alstom publication P2509 for complete detail). When a problem is detected, an alarm sounds and an on-screen description of the failure is presented.

3.4. OPERATING UNDER UNUSUAL CONDITIONS

The fail-safe design of the VPI II system allows continued operation in the presence of certain non-safety related faults. For instance, when a VPI II module indicates an abnormal or out-of-tolerance condition that has not caused a system shutdown. While continued operation may still be possible, the problem should be checked and corrected to avoid a possible complete system shutdown. Refer to P2511B, Volume 5, Maintenance and Troubleshooting for troubleshooting details.

3.5. OPERATIONAL CHANGES

If it becomes necessary to make changes to the VPI II control logic, authorized personnel should refer to Software Configuration, Heading 2.8.

WARNING

CHANGES TO CONTROL LOGIC CAN AFFECT SYSTEM SAFETY. IF ANY CHANGES ARE MADE TO THE VPI II CONTROL LOGIC, THE SYSTEM MUST BE TESTED TO VERIFY PERFORMANCE.

3.6. SHUTDOWN PROCEDURE

WARNING

DISRUPTION OF VITAL CONTROLLER SERVICE POSES A POTENTIAL THREAT TO RAIL SAFETY. BEFORE SHUTTING DOWN A FACILITY FOR ANY REASON, NOTIFY THE RAILROAD DISPATCHER IN CHARGE OF THE AFFECTED ROUTE(S). TAKE ALL STEPS NECESSARY TO ENSURE THE SAFE PASSAGE OF TRAFFIC IS MAINTAINED.

To shut down the VPI II system, set the system power supply switches to the OFF position. Power switches are typically located on or near the rack structure.

4. SECTION 4 – THEORY OF OPERATION

4.1. INTRODUCTION

This section provides an overview of VPI II system level functionality.

4.2. GENERAL

All VPI II boards (both Vital and non-vital) reside in a VPI II module. While the configuration of these modules can take many forms, a common interconnection system is used. All VPI II modules have the following interconnection structure:

- System Bus with P1 board connector (bottom connector)
- I/O Bus Motherboard with P2 board connector (middle connector)
 - Vital I/O Bus, or
 - Non-Vital I/O Bus, or
 - Expansion Bus (Expansion of System Bus) P3 board connector of I/O Bus Board (top connector)

Figure 4–1 illustrates a typical VPI II system that contains both Vital and non-vital elements and shows how they are interrelated. All four bus types are referenced in the figure.

4.3. VITAL SYSTEM OPERATION

To achieve fail-safe microprocessor-based interlockings, the VPI II processing system vitally verifies:

- inputs to the system are read correctly
- equations are evaluated correctly
- non-permissive outputs do not become permissive

Figure 4–2 shows the functional logic flow in a block diagram. Vital logic equations are written in Boolean form and are stored in the VPI II system Flash using Alstom's Computer-Aided Applications Programming Environment (CAAPE) software package. For details, refer to Alstom Publication P2512A or on-line manuals provided with the CAAPE package.

Vital input and output hardware is used in conjunction with a processing system controlled by safety software. Safety software is based on the principles of Safety Assurance Logic, an Alstom design philosophy applied to all products using microprocessors for Vital control. Additional techniques using Numerically Integrated Safety Assurance Logic (NISAL) are used to provide Vital processing logic that is compatible with the application-dependent logic required by the interlocking design.

VPI II primary logic performs the task of logically controlling the interlocking. The NISAL is integrated into the primary logic to prove that the intended tasks are performed correctly and to prove that no output can wrongly assert (for any reason) a permissive state.

When the CPU II board is used in conjunction with a CPU II Interface board (located on the DIN rails on the back of the processor), four additional serial ports are added to the Vital system.

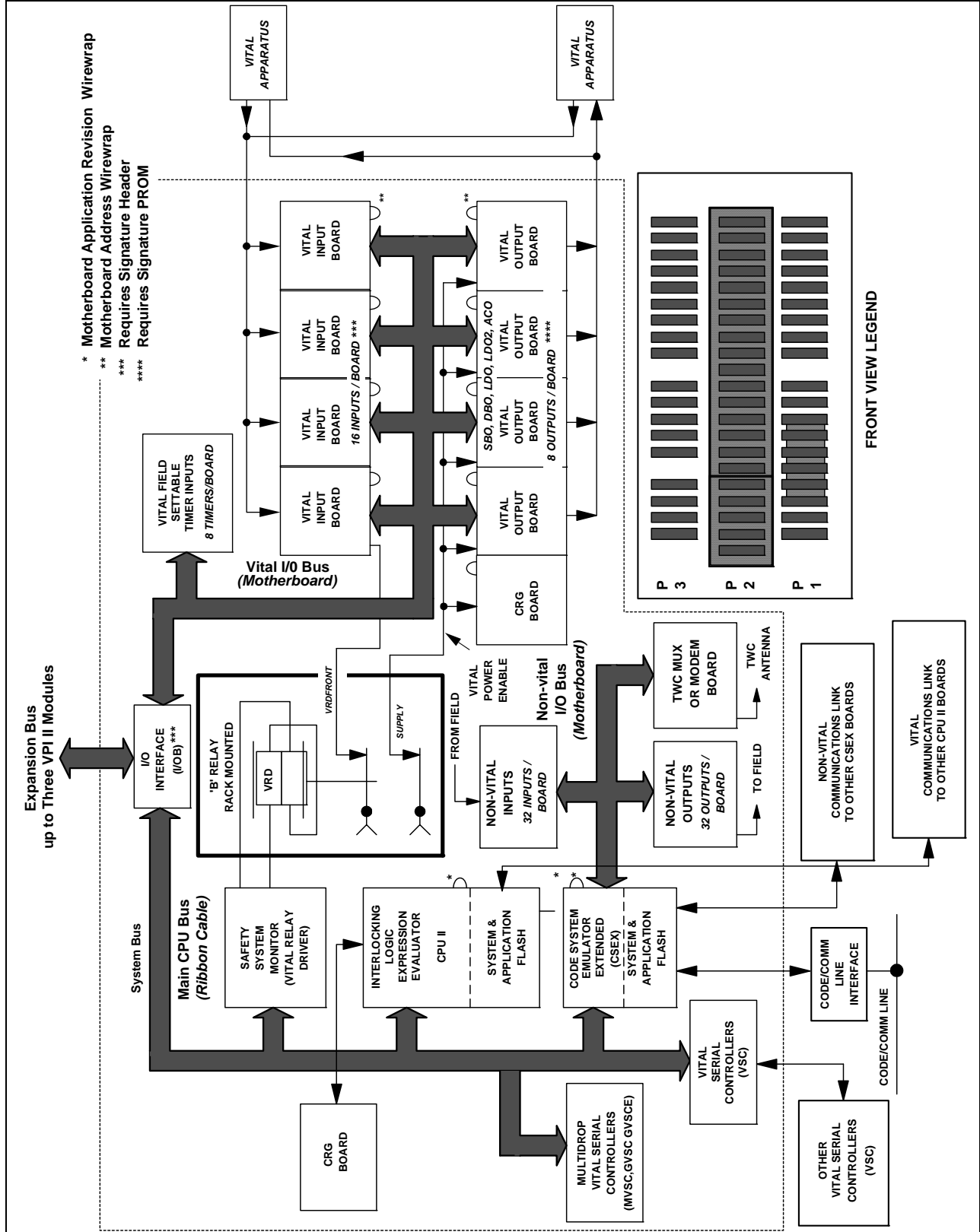


Figure 4-1. Typical VPI II System Configuration

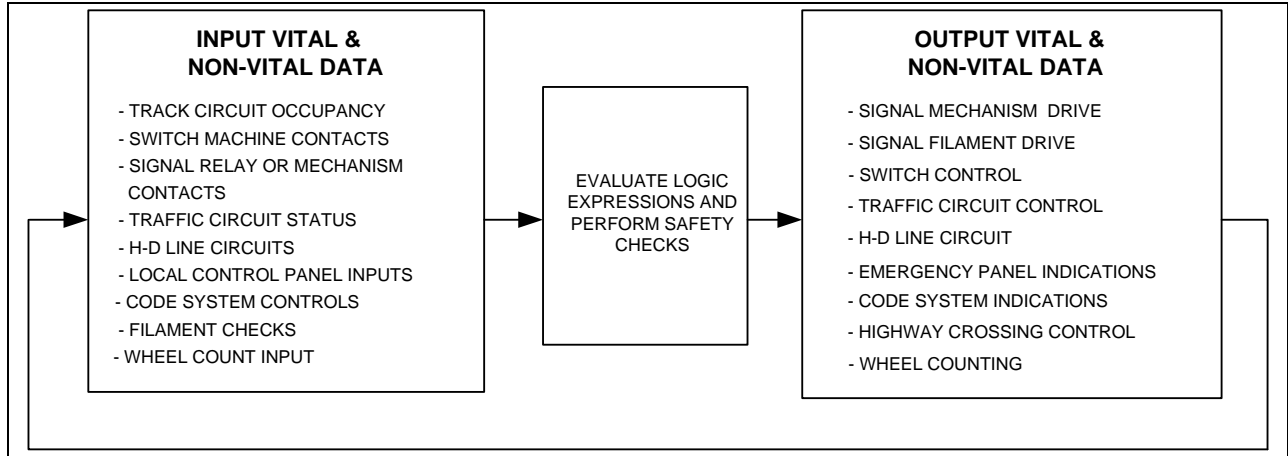


Figure 4–2. Functional Logic Flow

4.3.1. Vital Input Check Circuit

VPI II operation is based on a 1-second input-evaluate-output cycle. That is, every second all inputs are read, all equations are solved (using the read input values) and all outputs are updated based on the current evaluation. Vital hardware outputs are updated twice per second if they are flashing.

Figure 4–3 shows a simplified diagram of the Vital input check circuit. Each input is assigned a unique numerical value, or test word. During the input read process, this word is written to the input. The input circuit passes the word from the “data in” to “data out” terminals if, and only if, there is energy applied to the field terminals. The word returned to the CPU II for an “on” (true) or permissive input is the inverse of the serial word sent to the “data in” input. Any other word input is interpreted as “off” (false) or non-permissive. The read operation ensures that high levels of induced AC on the field conductors are not interpreted as a permissive input.

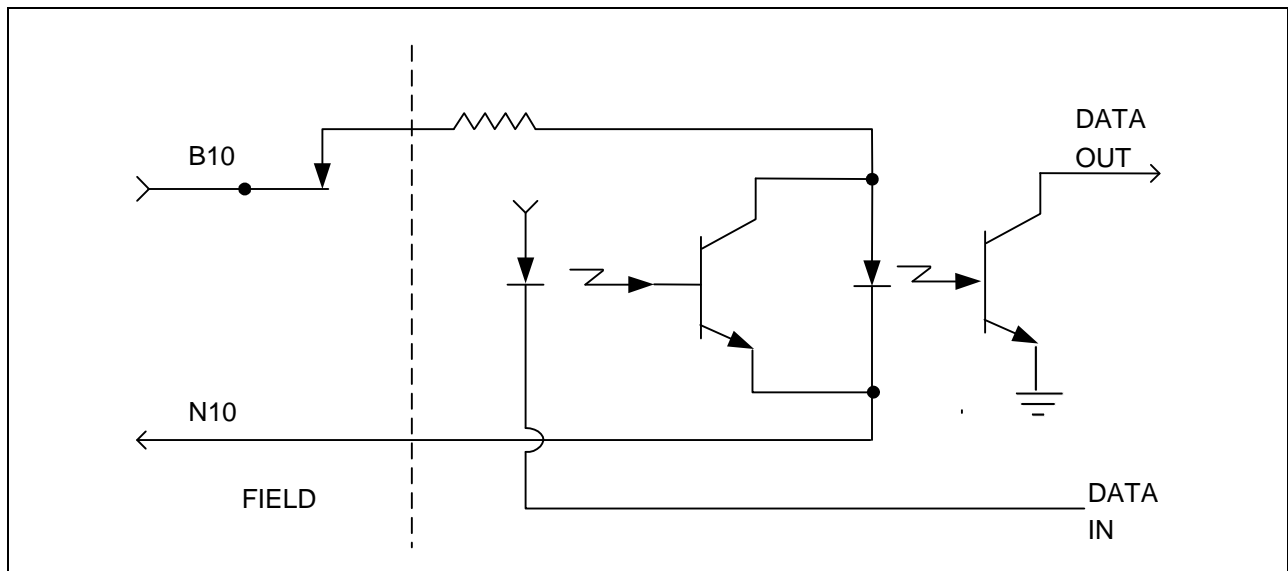


Figure 4–3. Vital Input Check Circuit

The data returned to the CPU II from each input is used in the expression (equation) evaluation. The input is read a second time using different data and the result of this process is used to solve a diverse set of expressions.

The field terminals for each Vital input circuit are electrically isolated from each other, so each input is equivalent to a separate, isolated Vital relay coil. Where a bipolar input function is required, two inputs may be interconnected in a “cross-coupled” arrangement. There are board assembly variations to handle different physical interface requirements.

4.3.2. Other Inputs

Vital serial input data (via the Vital Serial Controller board or via the Ethernet network) as well as non-vital input and code or communication system data via the CSEX board are obtained by the main processor once each second, and assigned true or false values in both channels.

4.3.3. Vital Expression Evaluation

Each Boolean expression is processed twice using diverse data in two separate processing channels. Each channel's result is unique. An example of a Boolean expression for a switch lock circuit is shown in Figure 4–4. In this example, the Vital output corresponding to the 1LR expression becomes true (energized) only if both channels' results combine to form a true value. This requires each of the three parameters to be true in both channels.

Expressions are evaluated by combining parameters mathematically using an algorithm based on polynomial division. The data result produced by this process is such that the correct values are only a small subset of possible values. They are different from other results in many bits (hamming distance) and exhibit a particular bit weight by the number of ones. This method produces a higher degree of security than does a simple logic scheme (AND, OR, ADD, etc.). All equations are executed diversely once per second and Vital precautions are taken to prevent skipping of expressions or evaluating out-of-order equations. In the equations shown in Figure 4–4, a plus (+) sign means an OR operation whereas a star (*) means an AND operation.

VPI II applies NISAL with a single microprocessor and a single set of software in combination with the system's primary function, a configured control system operates in a Vital manner without the need for redundant hardware or software. These concepts make extensive use of diversity and cycle checking to implement a safe function. Uniquely encoded checkwords are generated by the execution of Vital processes. Permissive outputs are allowed only if the full complement of generated checkwords is correct.

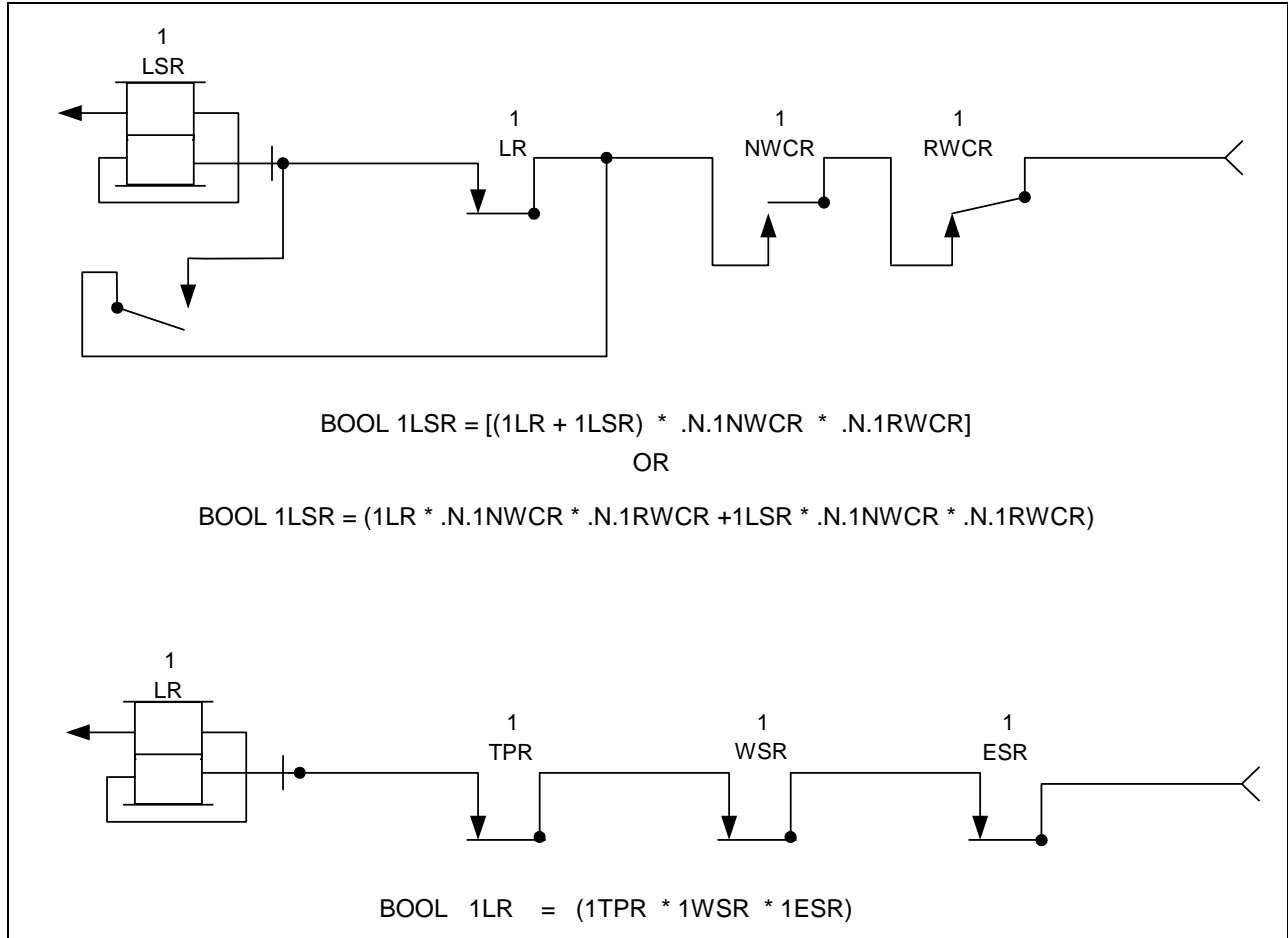


Figure 4–4. Boolean Expression Example (Switch Lock)

4.3.4. System Output Update

Results of the Vital expression evaluations set the Vital outputs to the evaluated states. Once per second, all system outputs are updated. Vital hardware outputs are updated twice every second if they are flashing. A set of independent checks is then run to ensure that only those outputs that evaluated true are in the permissive state. Output data for the non-vital outputs and the code/communication system indications are sent to the CSEX board once every second. Vital serial output messages are passed from the CPU II to the VSC boards and to the Ethernet network at the end of expression processing in each one-second cycle.

4.3.5. System Timing

An independently clocked reference timer performs most system timing and is separate from the processor clock. The reference timer is read “on the fly” to determine system timing. In addition, it is used to trigger processor interrupts at pre-defined intervals (for example, output check every 50 ms). Some checkwords are created based on timer contents. All checkwords are provided to a Vital Relay Driver (VRD) board for processing. Checkwords are only accepted once during a precise window that occurs in 50 ms intervals. If, and only if, all main and recheck checkwords are correct, delivered on time and are correct for the proper cycle is Vital energy supplied to the VPI II Vital outputs.

4.3.6. Absence-Of-Current Detector

A simplified version of an output circuit is shown in Figure 4–5. An Absence of Current Detector (AOCD) senses the current being delivered to the output load. If it is above a preset level (3 mA and 65 mA are typical depending on output type), the passage of a test word is blocked. Therefore, the only time that the correct data can pass from the Test Word Data In to the Test Word Data Out of the AOCD is if the current flow in the output is below the preset level. This provides a fail-safe means of verifying that an “off” output is indeed in the off state.

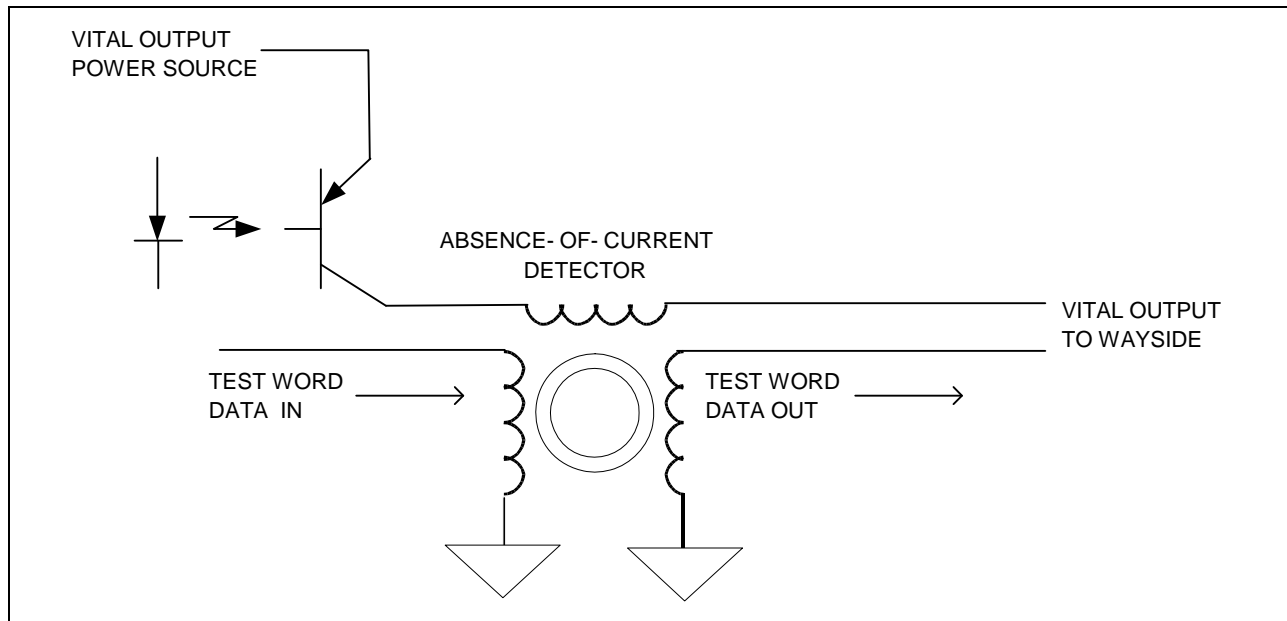


Figure 4–5. Absence-Of-Current Detector Circuit

The status of an output is positively known only when it is being checked. A unique serial data stream (word) is repeatedly applied to each AOCD for greater than 95% of each 50 ms recheck cycle. The resulting data from the AOCD is compressed in a shift register. The purpose of this operation is to obtain a numerical value for each output that is the mathematical equivalent of dividing the serial data stream by a primitive polynomial. The correct result for an “off” (false) occurs if, and only if, the current in that output is below the safe level for the entire check period. A unique numerical value is produced for each output.

The processor uses these values to create recheck checkwords and to maintain energy to the outputs. Using this method, the VPI II system can detect any output failure and vitally remove its power within a maximum of 140 ms (typically 100 ms).

4.3.7. Vital Checkwords

The VPI II system has two classifications of Vital checkwords. The recheck checkword set verifies the results from the state of all Vital outputs. The main checkword set verifies system operation with respect to processing equations, reading Vital inputs, timing and other internal operations.

The recheck checkword operates as follows. Every 50 ms, the state of each output is checked by creating a checkword that should correspond to its evaluated result. If an output is energized based on expression evaluation, then the true two-channel expression value is included in the formation of a checkword. If the output expression result is false, then a value returned from the Vital output check circuitry is used to prove that the output is off. This returned value is a unique result formed in two channels by circulating and compressing data continuously through the output check circuit. This data is then used to form a recheck checkword.

The main checkwords are used to vitally prove that the processes carried out by the Vital main cycle software are executed properly. These checkwords are created once per second.

Vital software processes include:

- Verification that all data used resulting in permissive outputs is current to that particular cycle; all old data must be vitally erased.
- Verification that routines and application information reside in memory as designed and are unaltered (signature analysis).
- Verification that all functions requiring strict timing (one-second processing cycle, 50 ms output recheck, Vital input timing, etc.) can be validated.

Memory buffers, which store system parameters, are erased each cycle by known benign data constants. A combination of these data constants, along with buffer address information, results in several of the main checkwords.

Signature analysis of system and application memory proves the integrity of stored FLASH data. Signature analysis results in higher error detection than does a simple checksum routine. The method of combining memory contents is similar to expression evaluation where an algorithm of polynomial division is used. The system and application memory is divided into blocks upon which a signature is calculated and used to create a main checkword.

4.3.8. Electrical Isolation

The Vital output circuitry achieves the same isolation and safety obtained from a Vital relay contact by:

- Maintaining physical separation between PC board traces and between connector pins
- Using opto-isolators, magnetic devices and other components that meet and/or exceed AAR isolation requirements

See P2511B, Volume 3, Vital Subsystem, for electrical isolation details on specific Vital boards.

4.3.9. Output Loads

The VPI II system can drive many different types of output loads. Different circuitry, therefore, is used to suit each application. The VPI II system can produce outputs that are equivalent to a single-break relay circuit, a double-break relay circuit, a lamp drive output and an AC output. The lamp drive output also includes circuitry for hot and cold filament tests. If a bipolar output function is required, double break output circuits may be interconnected in a cross-coupled arrangement to provide this function.

The following warning applies to the **SBO, DBO and ACO** VPI II board assemblies:

WARNING

LOW CURRENT VITAL OUTPUT BOARDS MAY FAIL WITH UP TO 3 MILLIAMPERES OF OUTPUT LEAKAGE CURRENT WITH THE SYSTEM REQUESTING THE OUTPUT TO BE IN THE DE-ENERGIZED STATE. TO PREVENT A POTENTIAL UNSAFE CONDITION, ANY LOAD DEVICE ATTACHED TO A LOW CURRENT VITAL OUTPUT CIRCUIT BOARD MUST NOT OPERATE AND MUST DE-ACTIVATE ABOVE 3 MILLIAMPERES. THIS INCLUDES ALL ENVIRONMENTAL OPERATING CONDITIONS AND ALL OPERATING VALUES OF THE LOAD DEVICE OVER ITS SERVICE LIFE. FAILURE TO FOLLOW THIS REQUIREMENT MAY LEAD TO UNEXPECTED OPERATION OF THE LOAD DEVICE.

The following warning applies to the following VPI II **LDO** and **LDO2** board assemblies:

WARNING

HIGH CURRENT VITAL OUTPUT BOARDS MAY FAIL WITH UP TO 65 MILLIAMPERES OF OUTPUT LEAKAGE CURRENT WITH THE SYSTEM REQUESTING THE OUTPUT TO BE IN THE DE-ENERGIZED STATE. TO PREVENT A POTENTIAL UNSAFE CONDITION, ANY LOAD DEVICE ATTACHED TO A HIGH CURRENT VITAL OUTPUT CIRCUIT BOARD MUST NOT OPERATE AND MUST DE-ACTIVATE ABOVE 65 MILLIAMPERES. THIS INCLUDES ALL ENVIRONMENTAL OPERATING CONDITIONS AND ALL OPERATING VALUES OF THE LOAD DEVICE OVER ITS SERVICE LIFE. FAILURE TO FOLLOW THIS REQUIREMENT MAY LEAD TO UNEXPECTED OPERATION OF THE LOAD DEVICE.

4.4. NON-VITAL SYSTEM OPERATION

The non-vital VPI II contains a number of circuit board types. A brief description of the boards used in the Non-Vital system is useful in understanding the integration of the non-vital VPI II into the overall ATC system. See P2511B, Volume 4, Non-Vital Subsystem, for a detailed description of each of the non-vital boards.

4.4.1. Non-Vital Processing

Version 3 and 4 Code System Emulator eXtended (CSEX3 and CSEX4) boards provide multi-port serial communications, along with Non-Vital logic capabilities.

The CSEX board is the Non-Vital equivalent of the Central Processor Board of the Vital VPI II system. It has a separate processor to serve the non-vital system. The CSEX board has serial data ports so it can directly interface with multiple communication environments and it controls non-vital I/O boards. The non-vital VPI II system can use multiple CSEX boards in one system. This allows division of some of the functions between boards, increasing system speed and capacity, while allowing a type of redundancy to be available. Furthermore, the CSEX board can simultaneously support multiple communication/code system protocols while performing non-vital application logic functions.

When the CSEX4 board is used in conjunction with a CSEX4 Interface board (located on the DIN rails on the back of the processor) additional serial ports and 2 Ethernet ports are added to the non-vital system.

4.4.2. Non-Vital TWC Communications

The NVTWC (Non-Vital Train-to-Wayside Communication) boards enable train-to-wayside and wayside-to-train messages as typically found in Transit applications. These messages pass from Central through the CSEX board, and then on to the train through the NVTWC Modem board and external antennae. Messages from the train to a Central Control can flow in the reverse direction. In addition, the messages to the train for loading train ID, dispatching, door control and performance levels are included. Various board assemblies exist for different physical interfaces.

4.4.3. Non-Vital I/O

The Non-Vital Input (NVI) board is used to detect discrete non-vital inputs. Discrete Non-Vital inputs are typically comprised of panel functions such as signal request, switch request, as well as miscellaneous inputs such as power off, ground detection and dwell timer program jumpers. For each of 32 inputs on a NVI board, an LED mounted near the board edge is used to represent the input state from the field equipment. Various board assemblies exist for different physical interfaces.

The Non-Vital Input Differential Switch (NVIDSW) board provides 32 isolated non-vital inputs to a VPI II system. Interface to the system is accomplished through the system motherboard. Input states are latched and then read every 25 ms. The NVIDSW board has 32 switches located on the front of the board that can be used to physically set the state of the inputs. The inputs can be forced ON, forced OFF or be the actual state of the physical input.

The Non-Vital Output (NVO) boards in a VPI II system are of two types, AC and DC. The AC NVO boards typically provide the panel lighting functions. The DC output boards are typically used to control panel lighting functions, to control other discrete non-vital outputs, and to drive any non-vital relays that are required. Various board assemblies exist for different physical interfaces.

The Non-Vital Relay Output (NVR) board provides 32 Form A non-vital relays interfaced through the system backplane to the connectors on the back of the module. The NVR board is functionally equivalent to its NVO predecessors. The outputs are grouped in four groups with 8 outputs each as on the NVO board, but the outputs on the P1 and P3 connectors are assigned two pins each: an even pin on the solder side of the board and an odd pin on the component side of the board. If the output is currently active, these two pins are connected through the associated relay contact, allowing current flow.

4.4.4. Non-Vital VPI II Diagnostics

Several types of diagnostics are available for the non-vital VPI II. As with Vital VPI II Printed Circuit Boards, edge mounted LEDs on each board give visual indications of board status. Also available for use as a diagnostic tool is a menu-driven series of diagnostic screens resident in the system software of the CSEX board and the NVTWC Modem board. These screens may be displayed on a VT100 video terminal connected to a 9-pin MAC (Maintenance ACcess) connector on the boards. An alternative means of viewing the diagnostics is through a PC with appropriate communications software capable of emulating a VT100 terminal on a PC, see Figure 4–6 for an example with a CSEX3 board. More information on Non-Vital board LEDs is provided in P2511B, Volume 4, Non-Vital Subsystem. See P2511V, Volume 5, Maintenance and Troubleshooting for Non-Vital Diagnostics via the MAC connector.

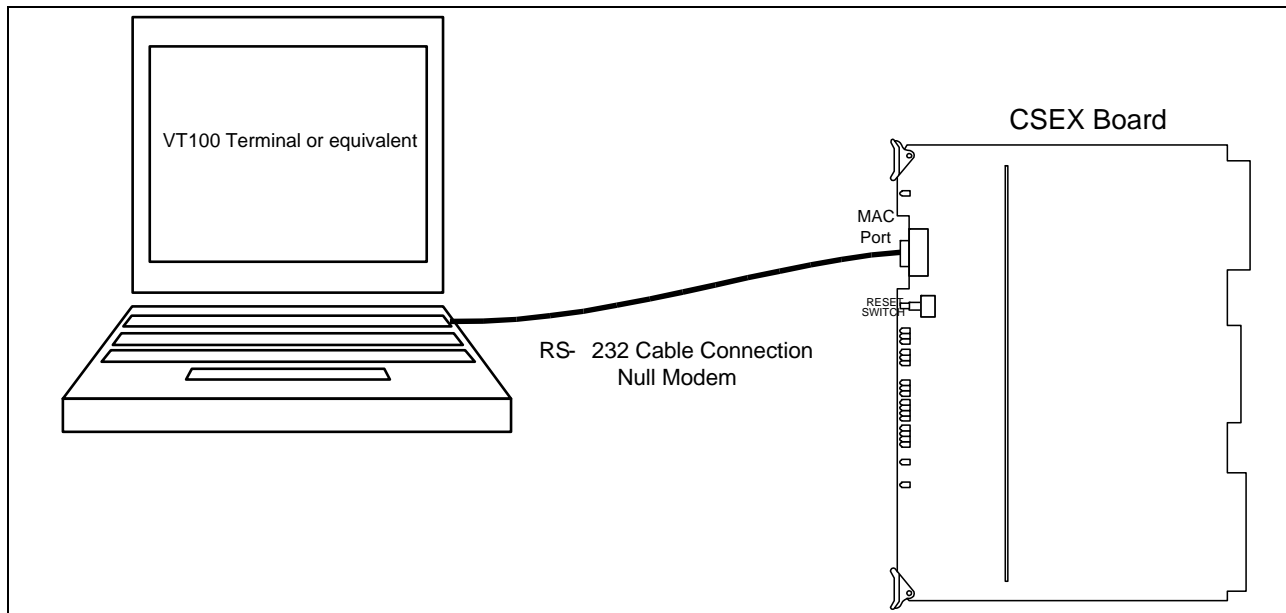


Figure 4–6. Example CSEX Diagnostic Connection

4.5. VPI II MODULE

Figure 4–7 shows the types of PC boards typically found in the VPI II module case (chassis). Slots are provided to hold up to 21 boards. Each Vital system must contain at least:

- 1 Central Processor Unit II (CPU II) board
- 1 Vital Relay Driver (VRD) board
- 1 Interface Bus (I/O Bus) board
- 1 Vital Input (DI) board
- 1 Vital Output (SBO, DBO, ACO, LDO or LDO2) board

These boards all operate on the System bus. A single VPI II system can consist of one to four modules.

The various boards that may be used in a VPI II configuration are summarized in Figure 4–7. For additional details regarding board combinations, see capacity Overview, Heading 2.3.

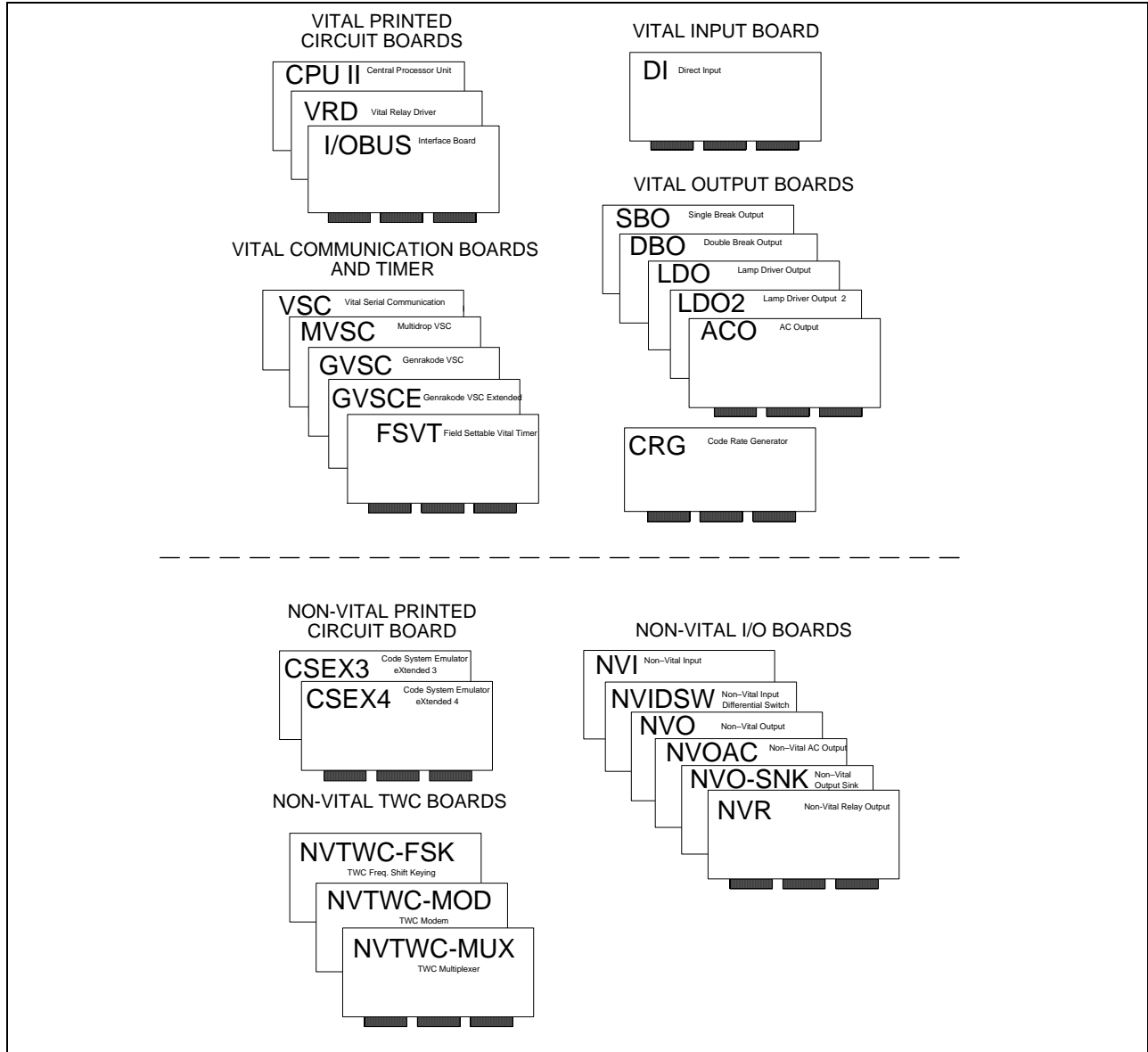


Figure 4–7. VPI II Boards Grouped by Vital and Non-Vital Functions

4.5.1. Board Placement

The following board placement rules apply to all Vital VPI II applications:

1. Modules containing Vital I/O must have an I/O Bus interface board.
2. Modules containing a CPU II board must have an I/O Bus interface board and a VRD board.
3. Modules containing non-vital I/O must have a CSEX board.

Figure 4–8 shows typical board placement in the VPI II module for most of the previously mentioned boards. The locations of individual boards in a VPI II configuration depend on the total complement of boards used.

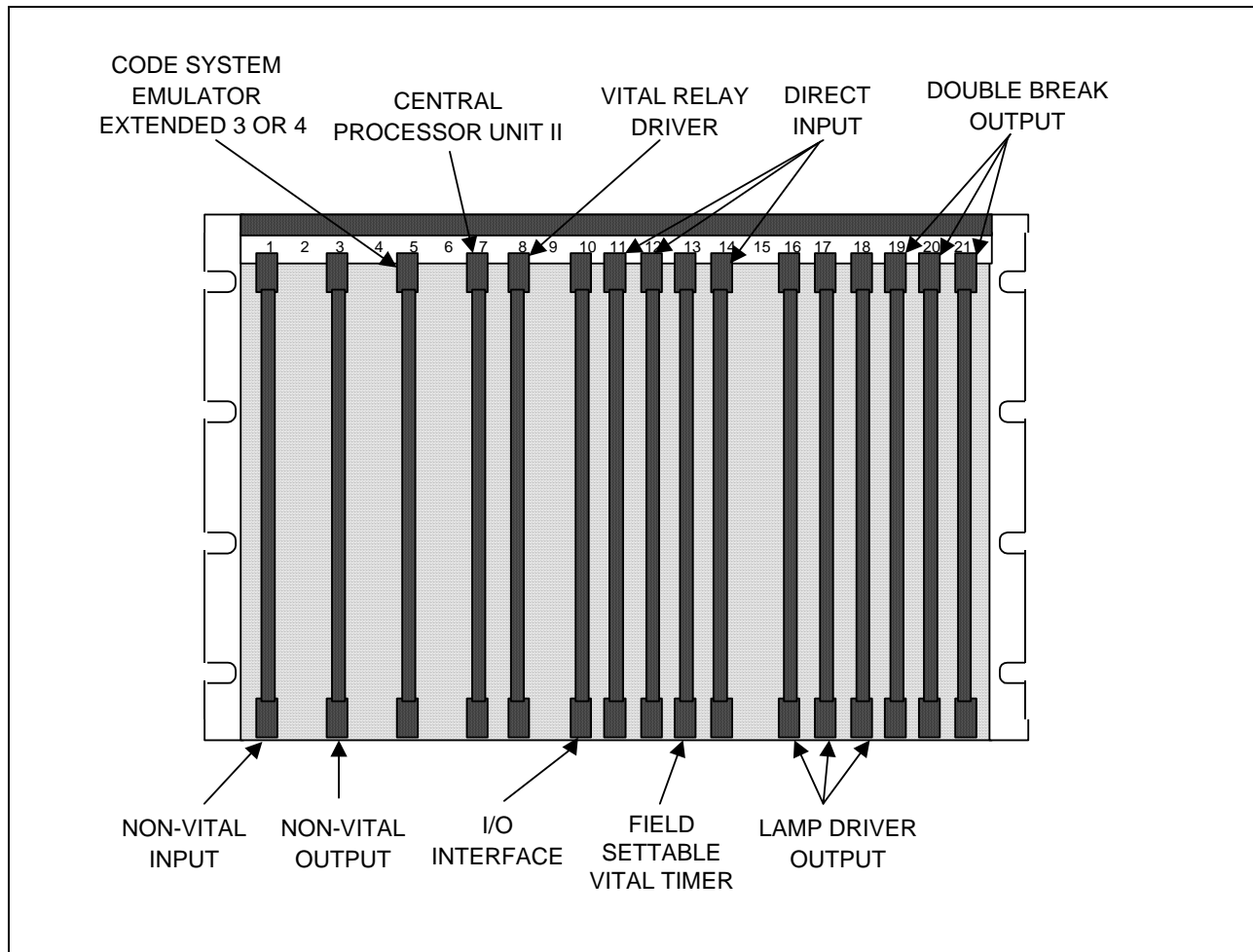


Figure 4–8. Typical Board Placement for Single Chassis VPI II System

In the System module, the Split Backplane Motherboard (P/N 59473-743-01) is typically used. This Motherboard has a split between slots 5 and 6 in order to create two independent I/O busses. Using this backplane, I/O boards may be housed in the same module. The I/O Bus Interface board controls the Vital I/O section of the Bus, while a CSEX4 board controls the non-vital I/O section of the bus. If the slots 1-5 are designated for Vital I/O, then slots 6-21 may be designated for non-vital I/O. Alternatively, if slots 1-5 are designated for non-vital I/O, slots 6-21 may be designated for Vital I/O. It is also possible to use the Split Backplane Motherboard to drive two separate Vital or two separate non-vital I/O sections.

If the system configuration requires more Vital or non-vital I/O than can be placed in a single module, additional Expansion modules can be used. These Expansion modules can use either the split backplane Motherboard (P/N 59473-743-01) as described above or a continuous backplane Motherboard (P/N 31166-166-01). However, when using a full complement of either all Vital or all non-vital boards in a System or Expansion module, the continuous backplane Motherboard that allows either an all Vital module or an all non-vital module must be used. The split backplane Motherboard allows mixing of Vital and non-vital I/O in the Expansion module.

The CPU II and VRD boards do not use the I/O bus and may be placed anywhere. The CPU II, VRD and I/O Bus interface boards are usually adjacent to each other to provide easy interconnection via the System Bus that interconnects their P1 connectors.

Some Vital boards may be used in the VPI II module in quantities of one or more. These are the:

- Direct Input (DI) board
- Single Break Output (SBO) board
- Double Break Output (DBO) board
- Lamp Driver Output (LDO or LDO2) board
- AC Output (ACO) board
- Vital Serial Communication (VSC) board
- Multidrop Vital Serial Communication (MVSC) board
- Genrakode Vital Serial Communication (GVSC) board
- Genrakode Vital Serial Communication Extended (GVSCE) board
- Field-Settable Vital Timer (FSVT) board
- Code Rate Generator (CRG) board

In addition, some combination of non-vital boards may be used in the module in quantities of one or more. These are the:

- Non-Vital Input (NVI) board
- Non-Vital Input Differential Switch (NVIDSW) board
- Non-Vital Output (NVO) board
- Non-Vital Relay Output (NVR) board
- Non-Vital AC Output (NVOAC) board
- Non-Vital Output Sink (NVO-SNK) board
- Non-Vital TWC Modem (NVTWC-MOD) board
- Non-Vital TWC Multiplexer (NVTWC-MUX) board
- Non-Vital TWC Frequency-Shift-Keying (NVTWC-FSK) board

Only 1 CSEX board can be used per module, but the system configuration can include up to four CSEX boards, depending on system design requirements. The additional communication emulation boards are located in expansion modules.

Figure 4–9 shows a typical VPI II module chassis. This chassis implements three different interface connector locations: P1, P2, P3 (P1 at bottom, P3 at top).

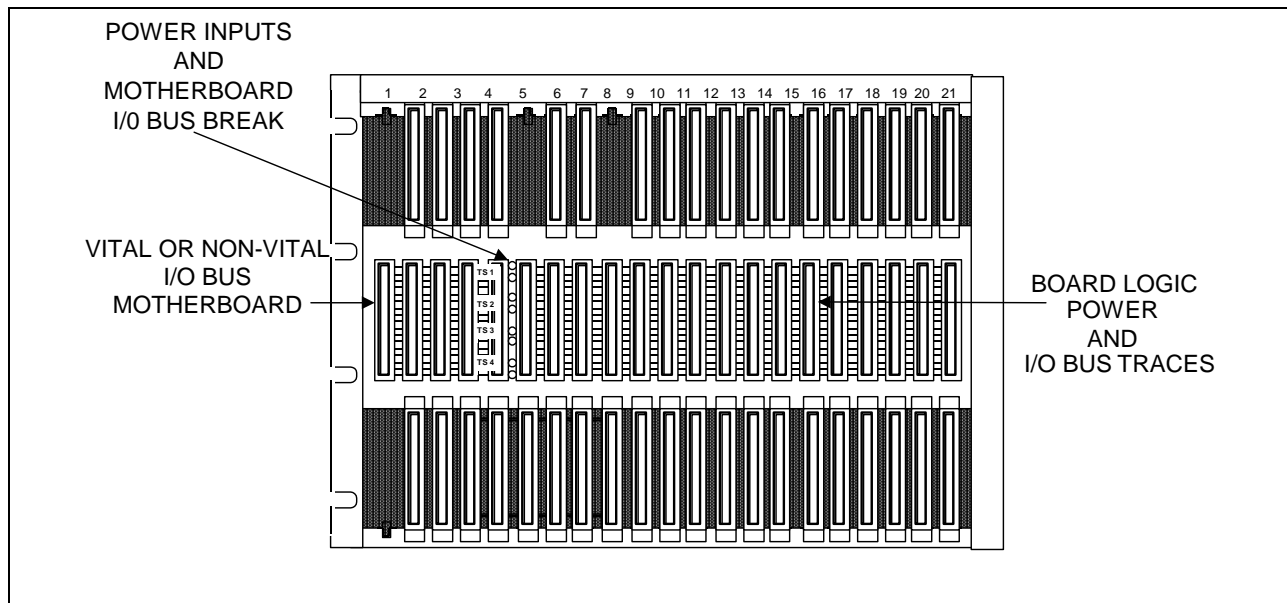


Figure 4–9. Typical VPI II Module Chassis

4.5.2. System Expansion

More than one module can be combined depending on the complexity of an application. The number of expansion modules that one system can handle depends on the quantity of Vital and non-vital I/O required and the number of Vital and non-vital equations that must be solved (the maximum number of expansion modules is three) for the application. For a description of VPI II capacity application guidelines see Capacity Overview, Heading 2.3

4.5.3. System Bus

The main CPU II is connected between the appropriate boards with a 60-way system bus ribbon cable (P/N 38216-395-XX). This cable interconnects the lower connector (P1) of each board with a system bus connection. The length of cable, number of connectors and location in the module is determined by the board layout for each application. Table 4–1 shows the interface connections to the Main System Bus.

A 7-position System Bus Motherboard (P/N 31166-201-XX) is also available for VPI II configurations. This motherboard is a double-sided board. It utilizes 60-way press-fit edge connectors and is designed to duplicate the functionality of the system bus ribbon cable (P/N 38216-395-XX) mentioned above. This System Bus Motherboard is located in connector row P1 and supports all the current system PC boards utilized on VPI II.

Table 4–1. System Bus Interface Connections

Pin	Description	Pin	Description
1	DB0	31	DT/R
2	5V COM	32	5V COM
3	DB1	33	ENIORD
4	DB2	34	5V COM
5	5V COM	35	ENIOWR
6	DB3	36	5V COM
7	DB4	37	AB18
8	5V COM	38	AB17
9	DB5	39	AB16
10	DB6	40	5V COM
11	5V COM	41	AB15
12	DB7	42	AB14
13	DB8	43	AB13
14	5V COM	44	5V COM
15	DB9	45	AB12
16	DBA	46	AB11
17	5V COM	47	AB10
18	DBB	48	5V COM
19	DBC	49	AB9
20	5V COM	50	AB8
21	DBD	51	AB7
22	DBE	52	5V COM
23	DBF	53	AB6
24	5V COM	54	AB5
25	MRD	55	AB4
26	5V COM	56	5V COM
27	MWT	57	AB3
28	5V COM	58	AB2
29	DEN	59	5V COM
30	5V COM	60	AB1

4.5.4. I/O Bus Motherboard (Vital I/O Bus And Non-Vital I/O Bus)

The Motherboard provides operating logic power and signal distribution to all boards in the module. This Motherboard can contain an all Vital I/O Bus, an all Non-Vital I/O Bus or a combination of both (with a split between slots 5 and 6). The I/O Bus Motherboard is connected to the P2 connector. Table 4–2 lists the I/O Bus Motherboard interface connections.

Table 4–2. Motherboard Interface Connections (Vital and Non-Vital)

Pin No.	Description (Vital I/O)	Description (Non-Vital I/O)
1	+5V	+5V
2	+5V	+5V
3	5V COM	5V COM
4	IODB0	NVDB0
5	IODB1	NVDB1
6	IODB2	NVDB2
7	IODB3	NVDB3
8	IODB4	NVDB4
9	IODB5	NVDB5
10	5V COM	5V COM
11	IODB6	NVDB6
12	IODB7	NVDB7
13	IODB8	EMSEL/
14	IODB9	NVA0
15	5V COM	5V COM
16	IODBA	NVA1
17	IODBB	NVA2
18	IODBC	NVA3
19	IODBD	NVA4
20	IODBE	NVA5
21	IODBF	NVA6
22	5V COM	5V COM
23	ENIORD/	NVIORD/
24	ENIOWR/	CLR.IREQ/

Table 4–2. Motherboard Interface Connections (Vital and Non-Vital) (Cont.)

Pin No.	Description (Vital I/O)	Description (Non-Vital I/O)
25	T-OUTC3	NVA7
26	TIMC4	NVA8
27	IOAB1	NVA9
28	IOAB2	NVA10
29	IOAB3	NVA11
30	IOAB4	NVA12
31	5V COM	5V COM
32	CLR/	NVA13
33	125 KHZ CLK	NVIOWR/
34	OUTC1/	POLL/
35	SEL DISABLE ON-OFF/ (See Note 1)	5V COM
36	DISABLE ON-OFF/	NVMRD/
37	IODT-R/	NVMWR/
38	5V COM	5V COM
39	RCHK CLK	INT/REQ/
40	SEL 1 (See Note 1,3)	NOT USED
41	OUTC2/	PROG
42	SEL 2 (See Note 1,3)	MISC SEL 2
43	SEL 3 (See Note 1)	MISC SEL 3
44	ADD SEL 0 (See Note 2)	ADD SEL 0 (See Note 2)
45	ADD SEL 1 (See Note 2)	(See Note 2)
46	ADD SEL 2 (See Note 2)	(See Note 2)
47	ADD SEL 3 (See Note 2)	(See Note 2)
48	5V COM	5V COM
49	+5V	+5V
50	+5V	+5V

Note 1: SEL 1 is wire-wrapped to SEL 2 to select the lower data bus and to SEL 3 to select the upper data bus, for use with Vital output boards. SEL DISABLE ON-OFF/ is wire-wrapped to pin 36 when a Vital output board requires special output checking. This function is used with the lamp drive outputs to permit hot and cold filament tests.

Note 2: Pins are wire-wrapped to 5V COM as required for the board address.

Note 3: For split motherboard, if slot 5/6 used for I/O, pins must be isolated.

4.5.5. Expansion Bus

The expansion bus is connected to the top connector (P3) of the System module's I/O Bus interface board and runs to a 60-way ribbon cable connector on the System module's rear panel. A 60-way ribbon cable (38216-404-XX) connects from the rear panel of the System module to the rear panel of the Expansion module(s). An internal 60-way ribbon cable then runs from the rear panel of the Expansion module(s) to the lower connector (P1) of the I/O Bus interface board and/or CSEX boards in the Expansion module(s).

If two or more Expansion modules are used, the Expansion bus is connected to one of the three remaining 60-way connector locations on the module's rear panel and then run to the other modules with additional 60-way ribbon cables. Connectors on the rear panel of the Expansion module(s) are used to implement this interconnection and to minimize the ribbon cable length.

4.5.6. Signature Header Assignments

All DI boards and their associated I/O Bus interface boards are assigned a Signature Header either automatically by the VPI II CAAPE package or manually by the Engineer. A Signature Header is a 36-pin header that is installed on DI and I/O Bus interface boards. Its purpose is to electrically key a specific PCB to a specific slot in the module. DI boards connected to different I/O Bus interface boards may have the same signatures. The signature is tied to the addressing for the I/O Bus interface and direct input boards and is used to prevent address failures from compromising system safety. There are 16 different signatures available for use by a system (P/N 59473-871-XX). Each of the 16 types is unique and plugs into sockets on each DI or I/O Bus interface board. See P2511B, Volume 3, Vital Subsystem, Appendix A for a complete list of Signature Headers and the associated Alstom part numbers.

4.5.7. Output Board Signature PROMs

Each Vital output board has an assigned Signature PROM (P/N 39780-003-XX) that contains the output check information for that board. Each PROM used in a system is unique. The PROM code required for each output board is assigned by the CAAPE package. This data is tied to a specific board address to prevent failures from compromising system safety. This 16-pin signature PROM plugs into a socket on each Vital output board to key the output board to a specific module slot. See P2511B, Volume 3, Vital Subsystem, Appendix A for a complete list of Signature PROMs and the associated Alstom part numbers.

An alternative assembly (P/N 31166-304-01) is available for the signature PROM. This assembly has two rotary selector switches that permit the assembly to be substituted for all possible signature PROMs by dialing the last two digits of the required PROM into the two switches. See Figure 4–10.

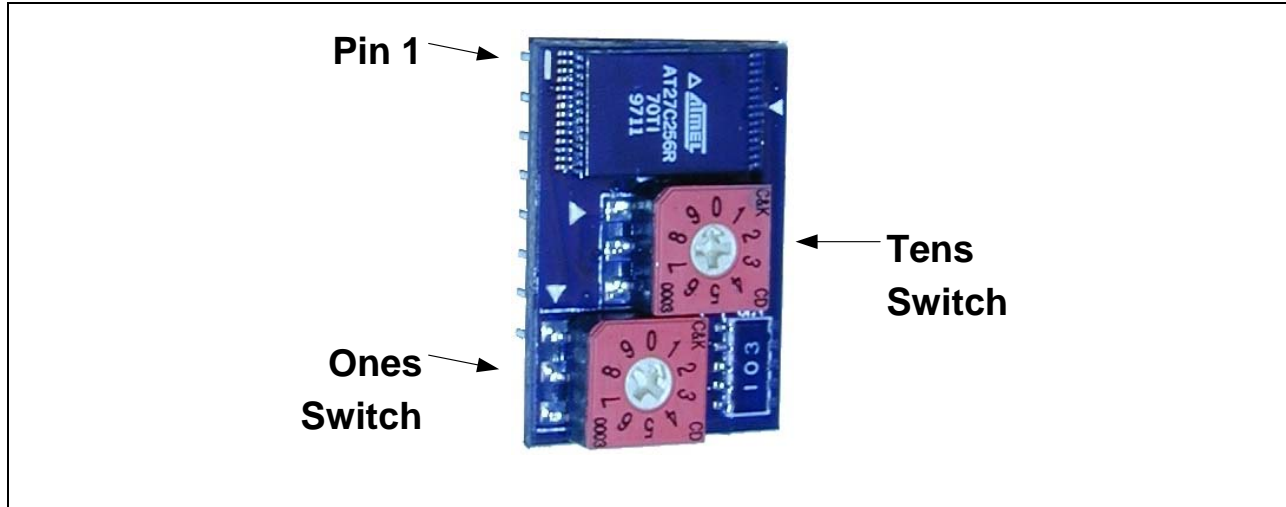


Figure 4–10. Rotary Selector Switches on P/N 31166-304-01

4.5.8. Board Address Assignments

Each board requires an address (except the CPU II board, which requires a revision signature on pins 42-47) that is encoded on the Motherboard. Motherboard pins 44, 45, 46, and 47 are used for this function. On the PC boards, these lines are connected to +5V through resistors, placing them in a high or “1” state. To set a particular line to a “0” state, the appropriate pin is wire wrapped or jumpered to 5-volt common on the Motherboard.

Motherboard pins are used to implement the desired address by wire wrapping or jumpering them to represent the binary equivalent of the address. Pin 44 represents the Least Significant Bit (LSB) of the address and pin 47 represents the most significant bit (MSB). For instance, board address "A," which is 1010 in binary, is implemented by wire wrapping pins 46 and 44 to 5-volt common. Board addresses are assigned by the CAAPE package. The CAAPE creates a list of the pins to be connected to 5-volt common by board slot as well as a module wire table.

For Vital output boards, additional connections are made. A wire wrap or jumper is installed to select the appropriate half of the Vital I/O bus allocated to a particular board (Motherboard pins 40, 42 and 43). There are 8 outputs on a board and the I/O bus is 16 data lines wide, so the CPU II controls any two output boards that have the same address. In this case, one is dedicated to the lower 8 data bus lines and the other to the upper 8 data bus lines. If special on/off checking of an output (such as for hot or cold filament check) is required, another wire wrap or jumper is installed (Motherboard pins 35 and 36). The VPI II CAAPE package defines the pins that are connected to create these functions.

4.5.9. Field-Settable Vital Timers

When using additional modules, all Field-Settable Vital Timer boards must be placed within the same module (always a system module) as well as the I/O Bus interface board (P/N 59473-827-XX) using signature A.

4.5.10. Power Supply Consideration

The logic circuitry portion of the VPI II module requires 5 VDC power. The common side of this supply is connected to the chassis, internal to the VPI II module. The chassis is electrically connected to the rack when it is properly mounted and the rack is connected to earth ground. When the normal signal battery is used with a DC/DC converter to create this supply, the converter must have 3000 VAC RMS isolation between input and output. Since the non-vital input and output boards do not maintain this isolation between the supply used for the non-vital I/O and the 5V power supply, supplies used for Vital circuits cannot be applied to the non-vital boards. When a system includes multiple VPI II modules connected together via the expansion bus, they may either have a common 5-volt power supply or have separate power supplies with their commons tied together. When separated power supplies are used, the output of each supply should be adjusted so that the modules are within 0.1 volt of each other. To guard against improper system operation, use of separate supplies must involve a single system power switch for all logic power.

The 5-volt supply must maintain an output between 4.75 and 5.25 volts as measured at the Motherboard or at the input power test points on the VPI II boards. Note that the number of boards installed in a VPI II module affects the total current drawn by the module. Maximum load specifications for each circuit board used in the VPI II module are given at the end of the board descriptions.

4.6. NON-VITAL SYSTEM AND COMMUNICATIONS SOFTWARE

The non-vital subsystem can simultaneously support multiple communication/code system protocols while performing non-vital input/output operations, application logic functions, train to wayside and wayside to train communications and data logging within the VPI II system. The data logged information is time-stamped and can be viewed real-time, can be selected by the user by run-time, or downloaded for off-line examination. The logic may be written using a combination of Boolean and higher-level programming techniques to control the communications and input/output functions.

4.6.1. I/O Application

Non-vital inputs and outputs can interface to external equipment in order to provide indications to a remote office or to an adjacent location. Outputs are capable of flashing at 60 cycles per second or 120 cycles per second. Examples of inputs and outputs include the following:

- Local Control Panel
 - Switch Machine Normal and Reverse Request Controls
 - Switch Machine Normal and Reverse Position and Lock Indications
 - Signal Request, Fleet and Cancel Controls
 - Signal Aspect and Fleeting Indications
 - Traffic Indications
 - Snow Melter - Controls and Indications
- Maintainer Calls
- Battery Power Alarms
- Ground Detection
- Fire Alarm
- Intrusion Alarm
- Room Temperature Monitor
- Track Indications
- System Health
- Redundancy Transfer

4.6.2. Logic Application

The non-vital logic can be written to perform a wide array of functions, including the following:

- N/X (Entrance/Exit) Interlocking Control
 - Controls provided from a local panel and/or a remote office
- Unilever Interlocking Control
- Remote Office Controls And Indications
- Train-to-Wayside and Wayside-to-Train Communications
 - Train Dwell Control
 - Train Identification
 - Train Berthing
- Automatic Train Operation
- Automatic Route Generation
- Auxiliary Train Tracking
- Interface to Vital Logic

4.6.2.1. Logic Statement Types

- Boolean Equations
- Timer Equations - delays the setting of an equation
- Integer Equations - arithmetic using variables and constants
- Program Flow Control: IF/ELSE, WHILE, GOTO
- User-Defined Subroutines: SUBROUTINE, CALL
- Predefined Subroutines: timer control, format conversion (e.g. Integer-Binary)
- Arrays

```

Queens1-NV.NV - Notepad
File Edit Search Help
BOOLEAN EQUATION SECTION

* SUBROUTINE TO COPY ARRAY BITS
SUBROUTINE COPY_BITS( BOOL BIT_ARRAY_1[],
                     BOOL BIT_ARRAY_2[],
                     INT NUM_BITS )

    COUNT = 0
    WHILE( COUNT < NUM_BITS )
    {
        BOOL BIT_ARRAY_2[COUNT] = BIT_ARRAY_1[COUNT]
        COUNT = COUNT + 1
    }
END COPY_BITS

* MAIN PROGRAM STARTS HERE
* WAIT FOR 10 SECONDS AFTER POWER-UP
TIME DELAY = 10 SECONDS
BOOL PWR_UP = TRUE
IF( PWR_UP==TRUE )
{
    * CHECK WHICH ARRAY TO COPY
    IF( MSG1_RECEIVED==TRUE && COPY_OK==TRUE )
        CALL COPY_BITS( SOURCE1,DEST,20 )
    ELSE
        CALL COPY_BITS( SOURCE2,DEST,20 )

    * USE PREDEFINED SUBROUTINE TO EXTRACT STATION NUMBER FROM
    * DEST ARRAY
    CALL BIN_TO_INT( STATION, DEST[0], DEST[1], DEST[2], DEST[3])
    IF( STATION==10 )
        BOOL STATION_10_SEND = SEND_OK * (.N.DEST[4] + URDFRNT-DI)
}

```

Figure 4–11. Logic Programming Sample

4.6.3. Communications

Alstom's library of communications protocols include:

- Office - This provides local or interlocking information to a remote office for display while allowing the office to control routing through the interlocking
- Remote Access Terminal
- Automatic Train Dispatch
- Platform Signs
- Intra- or Inter-system communications - Allow expansion of the system or partitioning of the non-vital subsystem into multiple processors; also allows neighboring locations to exchange interlocking information

A. APPENDIX A – GLOSSARY

A.1. INTRODUCTOPN

This appendix provides a glossary of the terms used in the 5 volumes of this manual set.

AAR	American Association of Railroads, replaced by AREMA
AC	Alternating Current
ACO	Vital AC Output board
ADV	Application Data Verifier
AF	Audio Frequency
Algorithm	A step-by-step procedure used to solve a problem
AOCD	Absence Of Current Detector
AREMA	American Railway Engineering and Maintenance of way Association
ARES	Advanced Railroad Electronic System
ATC	Automatic Train Control
ATCS	Advanced Train Control System
BBRAM	Battery-Backed RAM
BOM	Bill of Materials, a listing of the components that make up an assembly
Byte	This is a group of 8 bits handled as a unit
CAA	Computer Aided Application
CAAPE	Computer Aided Application Programming Environment
CIC	Cable Integrity Check
Clock	A device in a CPU that sends out electrical pulses at a fixed rate; the control unit uses the pulses to synchronize its operation

CMOS	Complementary Metal Oxide Semiconductor, a major class of integrated circuits; CMOS devices use little power and do not produce as much heat as other forms of logic
Compiler	Program that translates a high-level computer language into machine language
CPU	Central Processing Unit- the computer section that handles the actual processing of data into information
CRC	Cyclic Redundancy Checks
CRG	Code Rate Generator board
CSEX3	Code System Emulator eXtended board, version 3
CSEX4	Code System Emulator eXtended board, version 4
Data	Simply stated, it is another name for information
DBO	Double Break Output board
DC	Direct Current
Demultiplexing	The process of extracting a specific signal from a circuit carrying multiple (multiplexed) signals
DI	Direct Input board
Diagnostic	The process of detection and isolation of either a malfunction or mistake
Diagnostic Routine	A routine designed specifically to locate a malfunction in the computer
DIP	Dual In-line Package
DOT	Department Of Transportation
DPRAM	Dual-Ported Random Access Memory
Dual Port Memory	A shared memory (random access memory) that provides a mechanism for exchanging data between separate processor busses
DUART	Dual Universal Asynchronous Receiver/Transmitter
EMI	Electromagnetic Interference
Fail-Safe	The concept that if a system fails only a safe result will occur

Failure Mode	The effect by which a failure is observed, for example, short circuit
Firmware	Instructions stored on a ROM chip
Flash	A form of electrically erasable programmable read only memory used with embedded processors
FPGA	Field Programmable Gate Array
FRA	Federal Railroad Administration
FSVT	Field Settable Vital Timer board
GVSC	A specific Vital Serial Controller board (VSC) that provides a means of communicating to and from programmable Genrakode modules
GVSCE	A specific Vital Serial Controller board (VSC) that provides a means of communicating to and from programmable Genrakode modules
Handshaking Process	The exchange of predetermined signals for control purposes while establishing a connection between two data sets or modems; also, where predetermined arrangements of characters are exchanged by the receiving and transmitting equipment to establish synchronization
Hardware	The electronic section of the computer that stores and manipulates symbols under the direction of the computer
I/O	Input/Output
Initialization	The process of setting a circuit or portion of a circuit to a known state (typically on power-up or reset)
Interface	The equipment that enables one kind of hardware to be recognized and processed by another kind of hardware
Interrupt	The computer instruction that tells the computer to stop a program and do some other, more important task
IOB	Input/Output (I/O) Bus Interface board
Latch	A mode of operation for a circuit in which an output's state is maintained
LDO	Lamp Driver Output board
LED	Light-Emitting Diode
Logic Symbol	A symbol that graphically represents a logic element
LSB	Least Significant Bit

MAC	Maintenance ACESS connection point in a system; this enables the connection of a VT100 compatible terminal to examine system diagnostics and internal operation of the system
MMS	Maintenance Management System
MODBUS	A messaging structure used to establish master-slave/client-server communication between intelligent devices
Modem	A piece of equipment that connects data terminal equipment to a communication line
MOV	Metal Oxide Varistor, used for voltage surge suppression
MSB	Most Significant Bit
MUX	Multiplexer
MVSC	A specific Vital Serial Controller board (VSC) application that provides a means of communicating to and from AF Track Circuit modules
N/A	Not Applicable
NC	No Connection
NISAL	Numerically Integrated Safety Assurance Logic
Non-Vital	A component or function that is not critical to safety, its failure is not considered critical to the safe operation of a railroad but may be significant operationally
Non-Vital Circuit	This circuit provides either support or secondary services for the Vital networks; its failure is not considered critical to the safe operation of a railroad
NVI	Non-Vital Input board
NVIDSW	Non-Vital Input Differential Switch board
NVO	Non-Vital Output board
NVOAC	Non-Vital Output AC
NVO-SNK	Non-Vital Output Sink board
NVP	Non-Vital Processor board (CSEX for VPI II systems)
NVR	Non-Vital Relay Output board
NVTWC	Non-Vital Train to Wayside Communication

NVTWC-FSK	Non-Vital Train to Wayside Communication- FSK (Frequency Shift Keying) board
NVTWC-MOD	Non-Vital Train to Wayside Communication- MOD (Modem) board
NVTWC-MUX	Non-Vital Train to Wayside Communication-MUX (Multiplexer) board
PCB	Printed Circuit Board
PD	Polynomial Divider
Polynomial	A sum of two or more algebraic terms, each of which consists of a constant multiplied by one or more variables raised to a non-negative integral power
POR	Power On Reset
Port	A place of access to a device where energy may be supplied or withdrawn, or where the device may be observed or measured
Primordial	The logic rules applied to functions to be performed which assure safe operation
Processing	The conversion of raw data into usable information
Program	A series of instructions for the computer to follow
PROM	Programmable Read-Only Memory- programmable memory devices that store firmware
RAM	Random Access Memory- this part of memory temporarily stores information that is constantly being changed in the computer; here, words may be stored (written) or read (retrieved) in any order at random
Register	Where digital information is temporarily stored in a CPU or other digital logic device
Reset	It changes a bit value to zero or an output to an inactive condition
ROM	Read-Only Memory- this part of memory is built in during the manufacturing process; ROM stays intact even after the computer is turned off
RTC	Real-Time Clock
RTU	Relay Test Unit
SBO	Single Break Output board
Signature Header	Its purpose is to associate a type of board to its assigned position in the system; this device consists of a small plug-in printed circuit board or a PROM IC chip

Simulator	A special program that represents the behavior of a system
SMT	Surface Mount Technology
Software	Programs that direct the activity of the computer
SRAM	Static Random Access Memory
Subroutine	A section of a program that carries out a specific operation
Task	A program that is run as an independent unit
TTL	Transistor-Transistor Logic
TWC	Train-to-Wayside Communications
UART	Universal Asynchronous Receiver Transmitter
USART	Universal Synchronous/Asynchronous Receiver/Transmitter
Vital Component or Circuit	Any device, circuit or software module used to implement a Vital function; a Vital circuit is so named because its function is critical to the operation of certain signals and track equipment
Vital Function	A system, subsystem, equipment or component that provides a function critical to safety; it is implemented using fail-safe hardware and/or relays
VPI	Vital Processor Interlocking
VPI II	Alstom's Vital Processor Interlocking product
VRD	Vital Relay Driver board
VSC	Vital Serial Controller board that provides a means for exchanging the states of Vital interlocking functions between interlocking systems in a Vital manner
Watchdog Timer	A form of internal timer that is used to detect a possible malfunction; also, it is a timer set by a program to prevent the system from looping endlessly
Word	This is a group of two bytes
XOR	eXclusive OR

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